EE 435

Lecture 30

Data Converter Characterization

- Absolute Accuracy
- Relative Accuracy

DAC Design

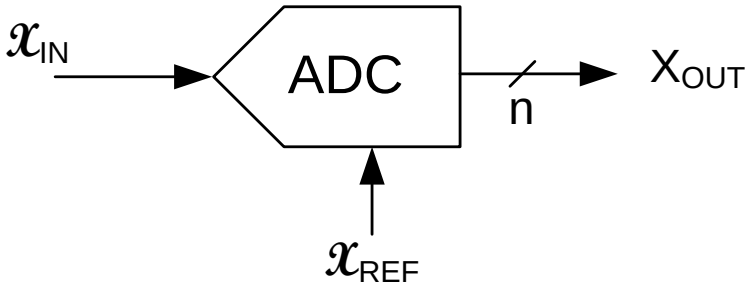
- The String DAC

Parasitics in MOS Devices

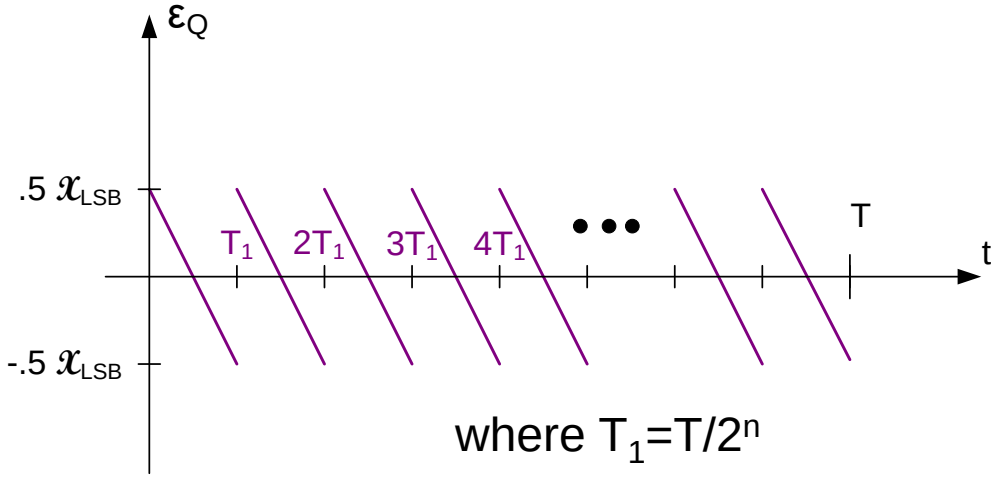
Quantization Noise in ADC

(same concepts apply to DACs)

Consider an Ideal ADC with first transition point at $0.5X_{LSB}$



If the input is a low frequency sawtooth waveform of period T that goes from 0 to X_{REF} , the error signal in the time domain will be:



where $T_1=T/2^n$

This time-domain waveform is termed the Quantization Noise for the ADC with a sawtooth (or triangular) input

Quantization Noise in ADC

$$E_{RMS} = \frac{x_{LSB}}{\sqrt{12}}$$

The signal to quantization noise ratio (SNR) can now be determined. Since the input signal is a sawtooth waveform of period T and amplitude X_{REF}, it follows by the same analysis that it has an RMS value of

$$x_{RMS} = \frac{x_{REF}}{\sqrt{12}}$$

Thus the SNR is given by

$$SNR = \frac{x_{RMS}}{E_{RMS}} = \frac{x_{RMS}}{x_{LSB}} = 2^n$$

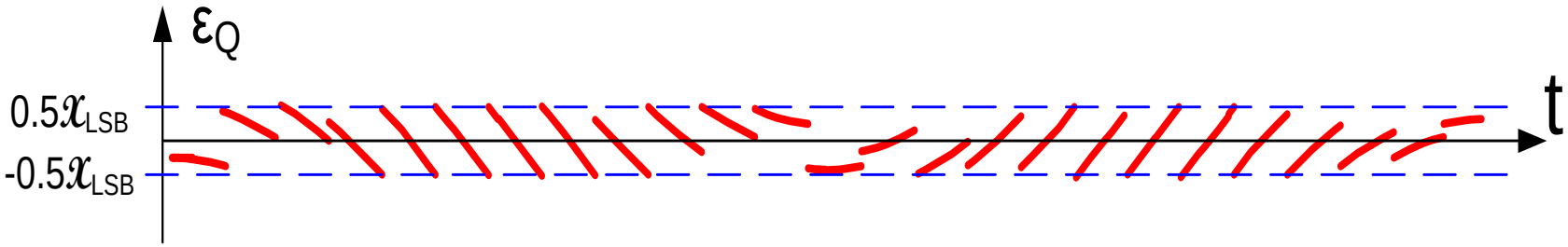
or, in dB,

$$SNR_{dB} = 20(n \bullet \log 2) = 6.02n$$

Note: dB subscript often neglected when not concerned about confusion

Quantization Noise in ADC

How does the SNR change if the input is a sinusoid that goes from 0 to x_{REF} centered at $x_{REF}/2$?



For low f_{SIG}/f_{CL} ratios, bounded by $\pm 0.5\ X_{LSB}$ and at any point in time, behaves almost as if a uniformly distributed random variable

$$\varepsilon_Q \sim U[-0.5X_{LSB}, 0.5X_{LSB}]$$

Quantization Noise in ADC

Recall:

If the random variable f is uniformly distributed in the interval [A,B]
f : U[A,B] then the mean and standard deviation of f are given by

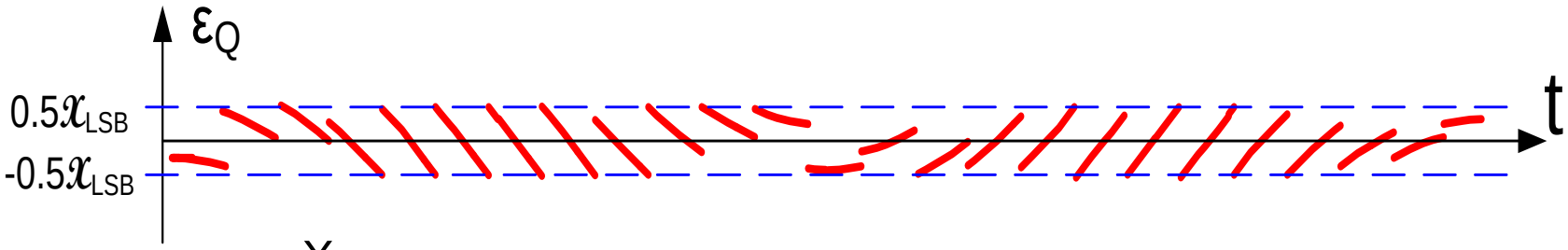
$$\mu_f = \frac{A+B}{2} \qquad \sigma_f = \frac{B-A}{\sqrt{12}}$$

Theorem: If n(t) is a random process and $\langle n(kT_S) \rangle$ is a sequence of samples of n(t) then for large T/T_S,

$$V_{RMS} = \sqrt{\frac{1}{T}\int_{t_1}^{t_1+T} n^2(t)\,dt} = \sqrt{\sigma^2_{n(kT_S)} + \mu^2_{n(kT_S)}}$$

Quantization Noise in ADC

How does the SNR change if the input is a sinusoid that goes from 0 to x_{REF} centered at $x_{REF}/2$?



$$V_{RMS} = \frac{X_{LSB}}{\sqrt{12}}$$

But $$V_{INRMS} = \left(\frac{X_{REF}}{2}\right)\frac{1}{\sqrt{2}}$$

Thus obtain

$$SNR = \frac{\frac{X_{REF}}{2\sqrt{2}}}{\frac{X_{LSB}}{\sqrt{12}}} = 2^n\sqrt{\frac{3}{2}}$$

Finally, in db,

$$SNR_{dB} = 20\log\left(2^n\sqrt{\frac{3}{2}}\right) = 6.02\,n + 1.76$$

ENOB based upon Quantization Noise Reference

Different factors can cause the SNR or SNDR of an ADC to not be ∞

- Quantization effects
- Device noise
- Interference Noise
- Nonlinear distortion
- Signal amplitude
- Jitter
- Computation errors
- …….

It is often useful to consider how an ADC performs from a SNR or SNDR viewpoint relative to how it would perform if only quantization effects (which are unavoidable) for an otherwise ideal ADC are present

An ENOB relative to an otherwise ideal ADC is often used as a metric for assessing SNR or SNDR performance

For example, consider a 14-bit ADC with a full-signal sinusoidal input that has quantization noise of $\frac{X_{LSB}}{\sqrt{12}} = 0.29X_{LSB}$, device noise with an RMS value of $2X_{LSB}$ and interference noise of 5 X_{LSB}. The total noise is then $5.4X_{LSB}$. Thus its SNR is equivalent to that of a much lower resolution ADC that has only quantization noise present. The resolution of that lower resolution ADC would be termed the ENOB relative to a Quantization Noise Only data converter

ENOB based upon Quantization Noise Reference

$$SNR_{dB} = 6.02\,n + 1.76$$

Solving for n, obtain

$$ENOB = \frac{SNR_{dB} - 1.76}{6.02}$$

Note: could have used the SNR_{dB} for a triangle input and would have obtained the expression

$$ENOB = \frac{SNR_{dB}}{6.02}$$

But the earlier expression is more widely used when specifying the ENOB based upon the noise level present in a data converter

Quantization Noise

Example: If a 14-bit audio output is derived from a DAC designed for providing an output of 100W but the normal listening level is at 50mW, what is the SNR due to quantization noise at maximum output and at the normal listening level? What is the ENOB of the audio system when operating at 50mW?

At 100W output, SNR=6.02n+1.76 = 86.04dB

$$\frac{V^2}{R_L}=100W \qquad \frac{V_1^2}{R_L}=50mW \qquad V_1=\frac{V}{44.7}$$

$$20\log_{10}V_1=20\log_{10}V-20\log_{10}44.7= \ -33dB$$

At 50mW output, SNR reduced by 33dB to 53.04dB

$$ENOB = \frac{SNR_{dB}-1.76}{6.02} = \frac{53.04-1.76}{6.02} = 8.51$$

Note the dramatic reduction in the effective resolution of the DAC when operated at only a small fraction of full-scale.

Performance Characterization of Data Converters

- Static characteristics
  - Resolution
  - Least Significant Bit (LSB)
  - Offset and Gain Errors
  - Absolute Accuracy
  - Relative Accuracy
  - Integral Nonlinearity (INL)
  - Differential Nonlinearity (DNL)
  - Monotonicity (DAC)
  - Missing Codes (ADC)
  - Quantization Noise
  - Low-f Spurious Free Dynamic Range (SFDR)
  - Low-f Total Harmonic Distortion (THD)
  - Effective Number of Bits (ENOB)
  - Power Dissipation

Absolute Accuracy

Absolute Accuracy is the difference between the actual output and the ideal or desired output of a data converter

The ideal or desired output is in reference to an absolute standard (often maintained by the National Institute of Standards and Technology (NIST) formerly Bureau of Standards) and could be volts, amps, time, weight, distance, or one of a large number of other physical quantities)

Absolute accuracy provides no tolerance to offset errors, gain errors, nonlinearity errors, quantization errors, or noise

In many applications, absolute accuracy is not of a major concern

but … scales, meters, etc. may be more concerned about Absolute accuracy than any other parameter

Relative Accuracy

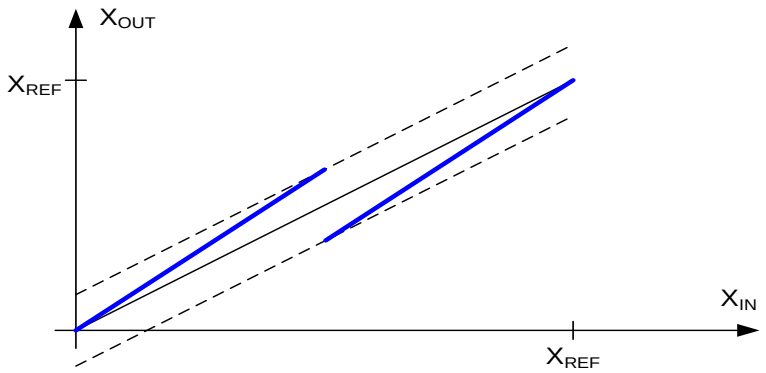
In the context of data converters, pseudo-static Relative Accuracy is the difference between the actual output and an appropriate fit-line to overall output of the data converter

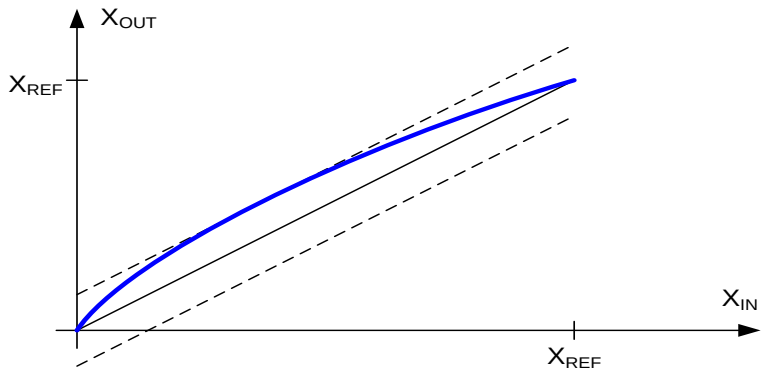
INL is often used as a measure of the relative accuracy

In many, if not most, applications, relative accuracy is of much more concern than absolute accuracy

Some architectures with good relative accuracy will have very small deviations in the outputs for closely-spaced inputs whereas others may have relatively large deviations in outputs for closely-spaced inputs

DNL provides some measure of how outputs for closely-spaced inputs compare





DAC Architectures (Nyquist Rate)

Types

- Voltage Scaling
  - Resistor String DACs (string DACs)
  - Interpolating
- Current Steering
  - Binarily Weighted Resistors
  - R-2R Ladders
  - Current Source Steering
    - Thermometer Coded
    - Binary Weighted
    - Segmented
- Charge Redistribution
  - Switched Capacitor
- Serial
  - Algorithmic
  - Cyclic or Re-circulating
  - Pipelined
- Integrating
- Resistor Switching
- MDACs (multiplying DACs)

DAC Architectures

Structures

- Hybrid or Segmented
- Mode of Operation
  - Current Mode
  - Voltage Mode
  - Charge Mode
- Self-Calibrating
  - Analog Calibration
    - Foreground
    - Background
  - Digital Calibration
    - Foreground
    - Background
  - Dynamic Element Matching
- Laser of Link Trimmed
- Thermometer Coded or Binary
- Radix 2 or non-radix 2
- Inherently Monotone

DAC Architectures

- Type of Classification may not be unique nor mutually exclusive
- Structure is not mutually exclusive
- All approaches listed are used (and probably some others as well)
- Some are much more popular than others
  - Popular Architectures
    - Resistor String (interpolating)
    - Current Source Steering (with segmentation)
- Many new architectures are possible and some may be much better than the best currently available
- All have perfect performance if parasitic and matching performance are ignored !
- Major challenge is in determining appropriate architecture and managing the parasitics

Nonideal Effects of Concern

- Matching
- Parasitic Capacitances
  (including Charge injection)
- Loading
- Nonlinearities
- Interconnect resistors
- Noise
- Slow and plagued by jitter
- Temperature Effects
- Aging
- Package stress

Observations

- Yield Loss is the major penalty for not appropriately managing parasitics and matching and this loss can be ruthless
- The ultimate performance limit of essentially all DACs is the yield loss associated with parasitics and matching
- Many designers do not have or use good statistical models that accurately predict data converter performance
- If you work of a company that does not have good statistical device models
  - Convince model groups of the importantc of dedveloping these models
  - (or) develop appropriate test strutures to characterize your process
- Existing nonlinear device models may not sufficiently accurately predict device nonlinearities for high-end data converter applications

Observations

- Experienced Designers/Companies often produce superior data converter products
- Essentially all companies have access to the same literature, regularly reverse engineer successful competitors products and key benefits in successful competitors products are generally not locked up in patents
- High-end designs(speed and resolution) may get attention in the peer community but practical moderate performance converters usually make the cash flow
- Area (from a silicon cost viewpoint) is usually not the driving factor in high-end designs where attractive price/mfg cost ratios prevail

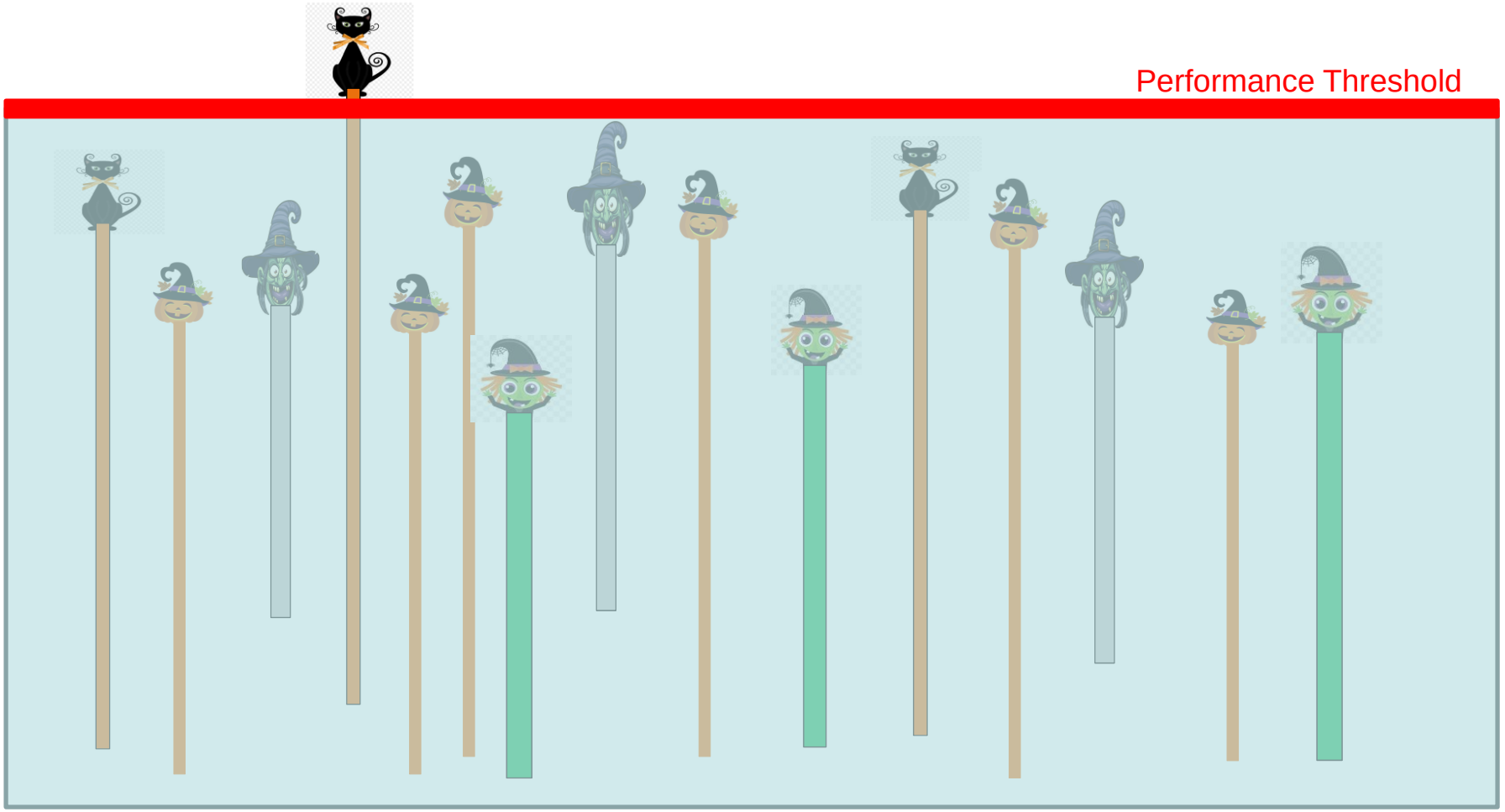
Data Converter Design Strategies

- There are many different DAC and ADC architectures that have been proposed and that are in widespread use today
- Almost all work perfectly if all components are ideal
- Most data converter design work involves identifying the contributors to nonideal performance and finding work-arounds to these problems
- Some architectures are more difficult to find work-arounds than others
- All contributors to nonidealities that are problematic at a given resolution of speed level must be identified and mitigated
- The effects of not identifying nonidealities generally fall into one of two categories
  - Matching-critical nonidealities (degrade yield)
  - Component nonlinearities (degrade performance even if desired matching is present)

Data Converter Design Strategies

Remember:

Need to keep nonideal effects below an acceptable performance threshold



Identifying Problems/Challenges and Clever/Viable Solutions

- Many problems occur repeatedly so should recognize when they occur
- Identify clever solutions to basic problems – they often are useful in many applications
- Don't make the same mistake twice !

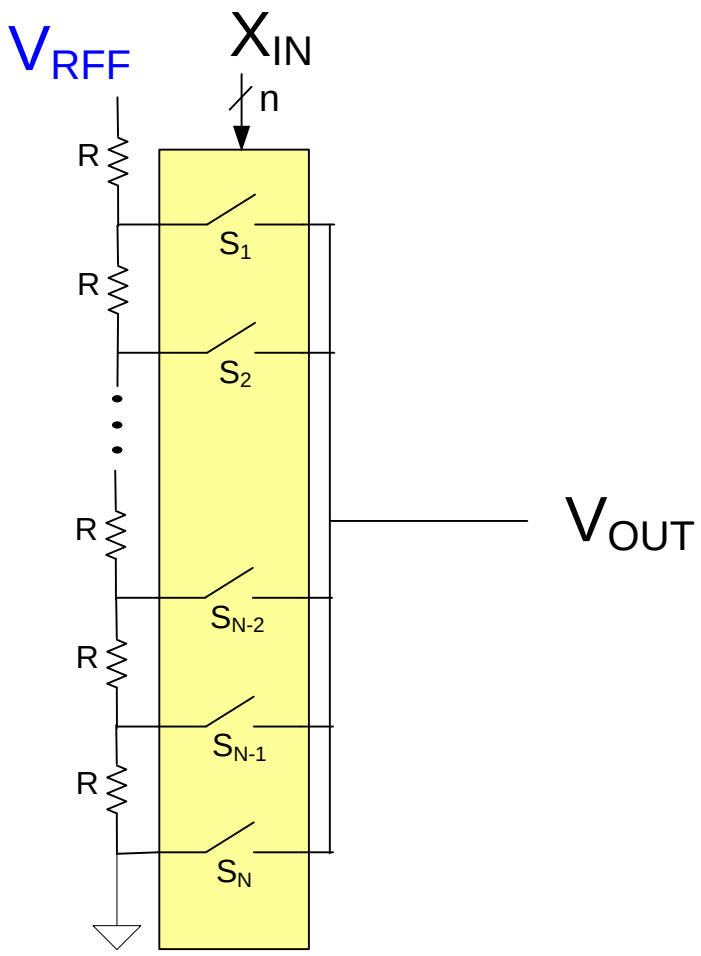
The problem:

The perceived solution:

The practical or clever solution:

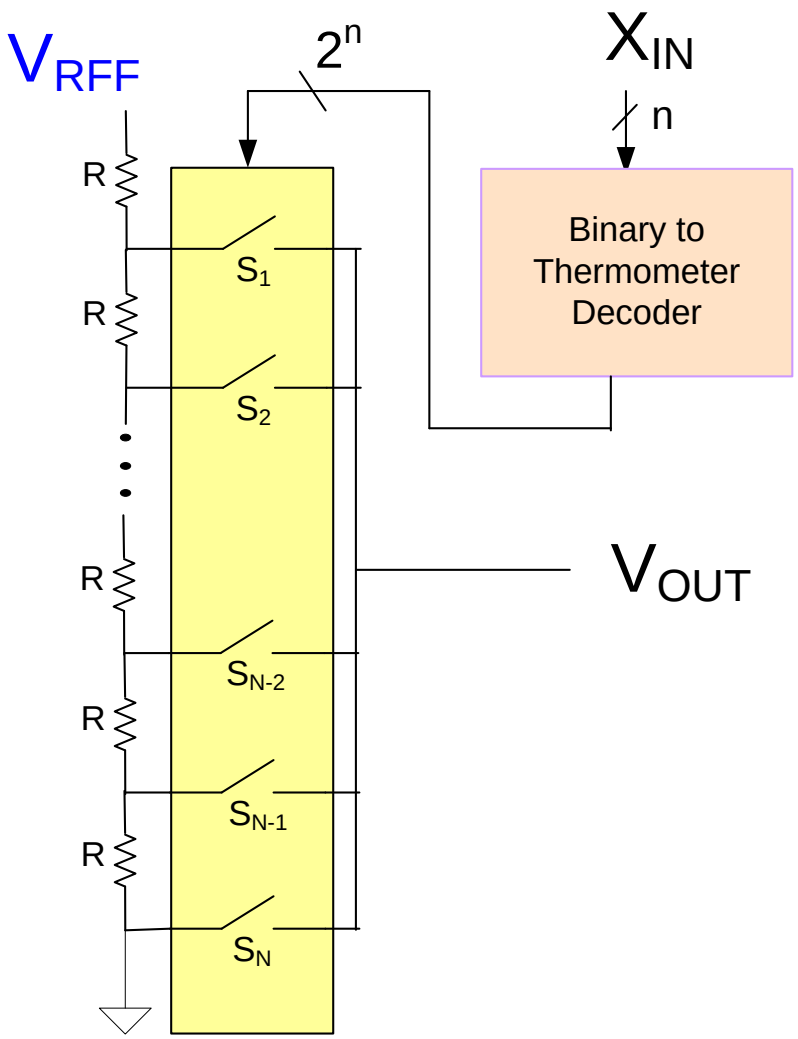
Keep A List !

R-String DAC



Basic R-String DAC

R-String DAC



Basic R-String DAC including Logic to Control Switches

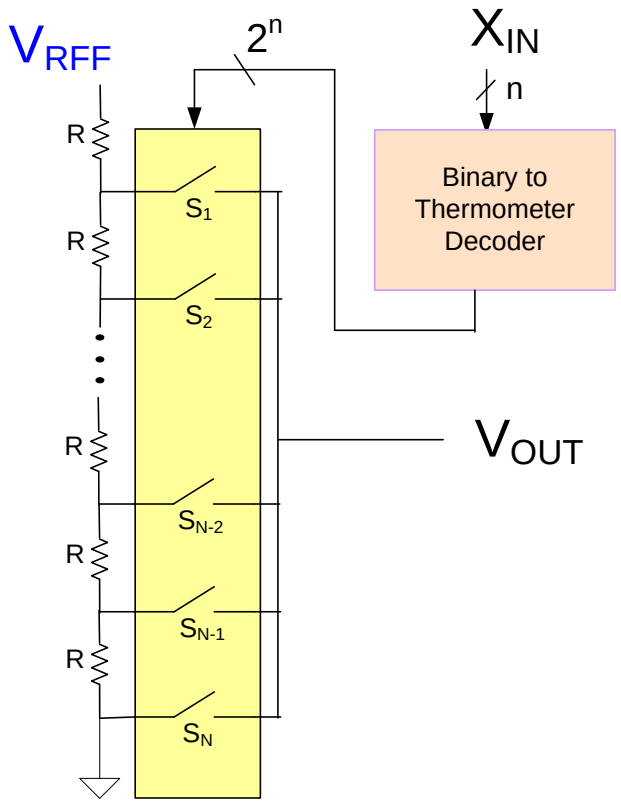
R-String DAC

If all components are ideal, performance of the R-string DAC is that of an ideal DAC!

Key Properties of R-String DAC

- One of the simplest DAC architectures
- R-string DAC is inherently monotone

Possible Limitations or Challenges



R-String DAC

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- One of the simplest DAC architectures
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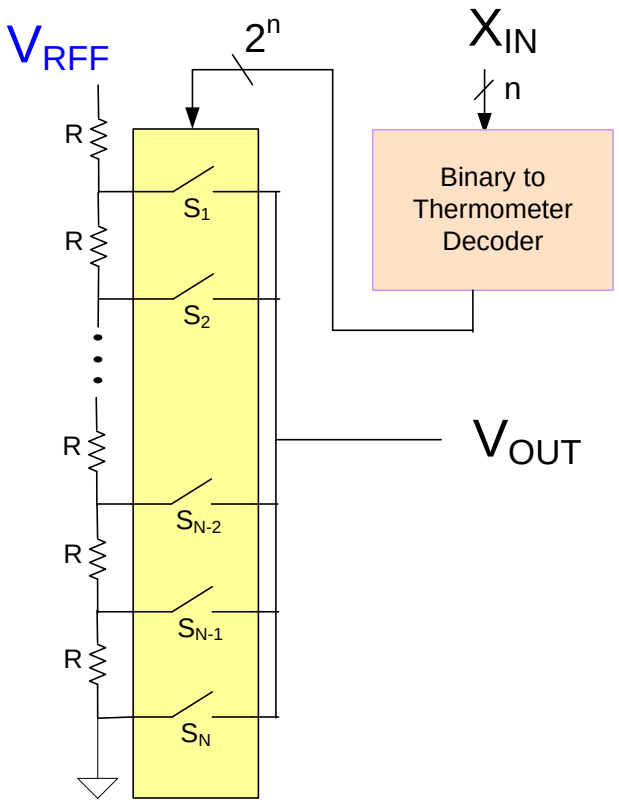
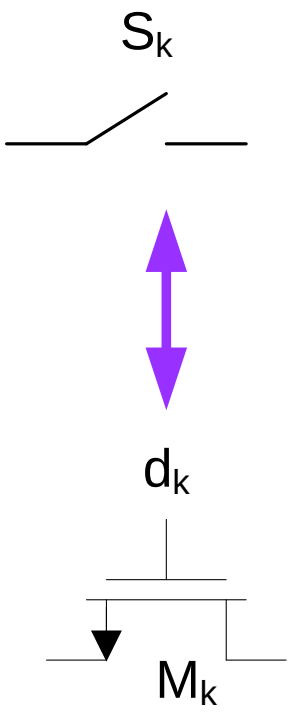
Possible Limitations or Challenges

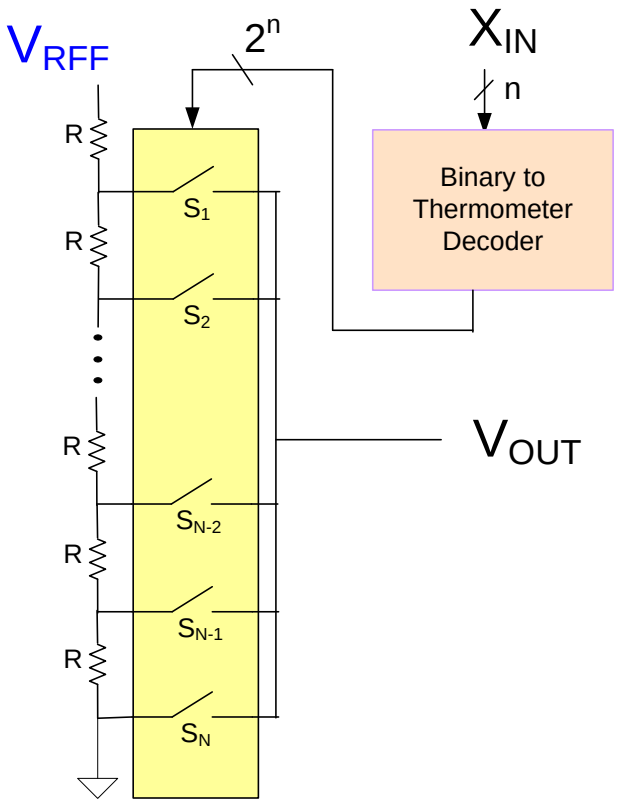
- Binary to Thermometer Decoder (BTTD) gets large for n large
- Logic delays in BTTD may degrade performance
- Matching of the resistors may not be perfect
  - Local random variations
  - Gradient effects
- How can switches be made ?



R-String DAC

Typical strategy for implementing the switch



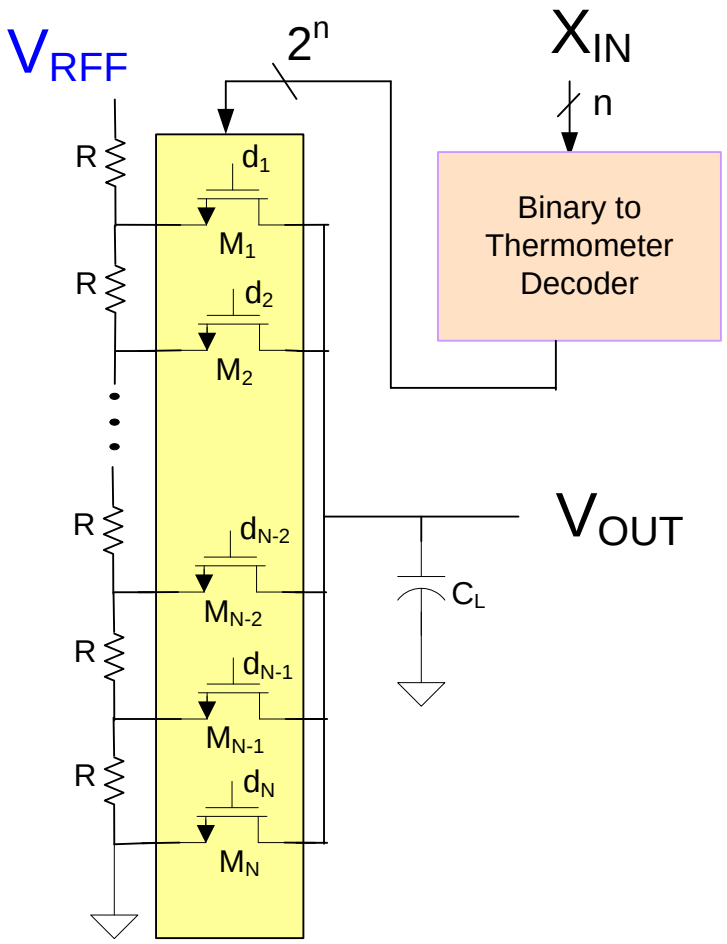


- **Switch array is an analog MUX**
- **Very simple structure**
- **Switch array combined with the BTTD forms a 2^n:1 analog MUX**

R-String DAC

R-String DAC with MOS switches

Possible Limitations:



R-String DAC

R-String DAC with MOS switches

Possible Limitations:

Switch impedance is not 0

Switch may not even turn on at all if V_{REF} is large

Switch impedance is input-code dependent

Time constants are input-code dependent

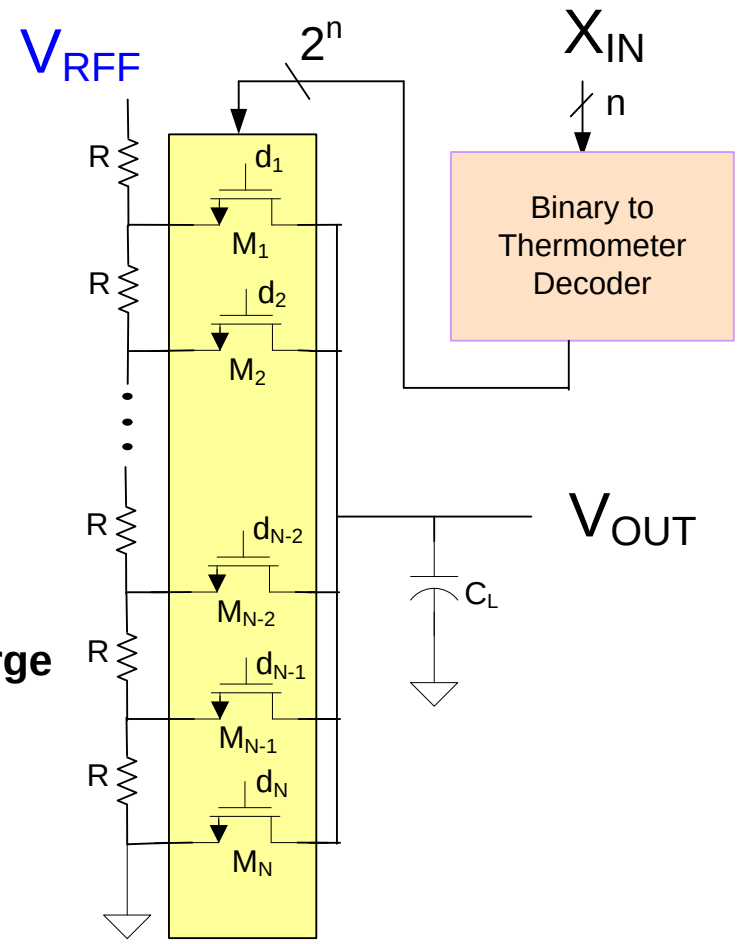
Transition times are previous-code dependent

C_L has 2^n diffusion capacitances so can get very large
(will discuss this issue next)

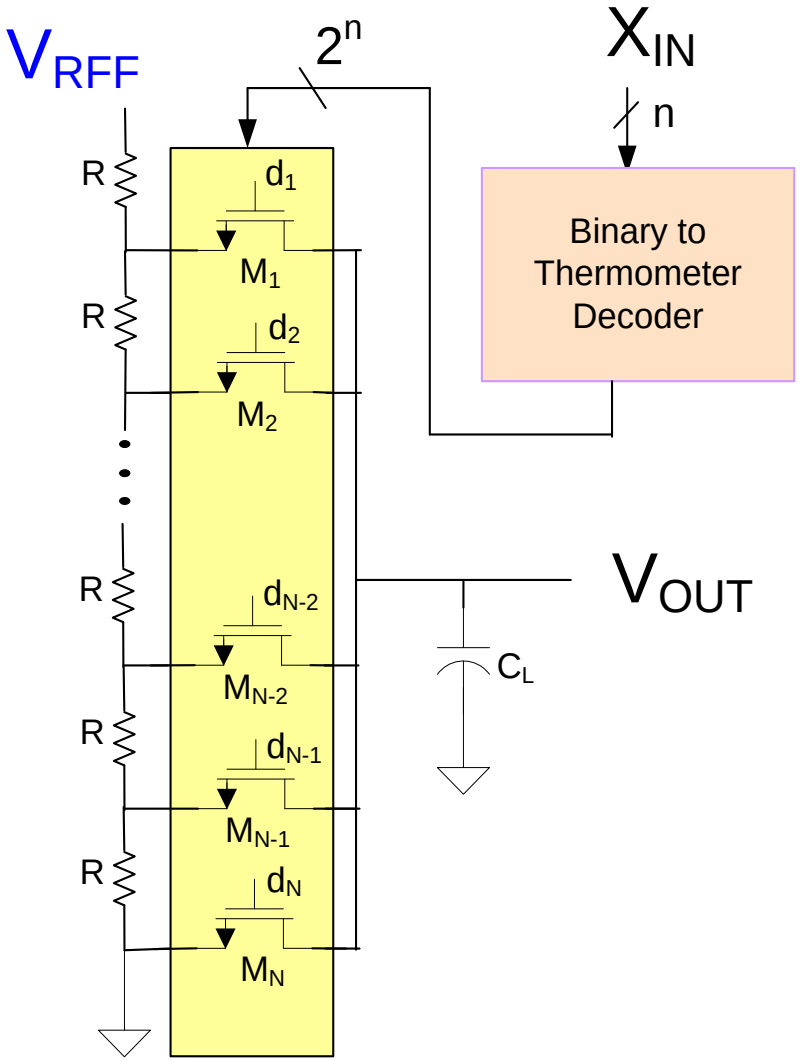
Mismatch of resistors
- **local random variation**
- **gradient effects**

Decoder can get very large for n large

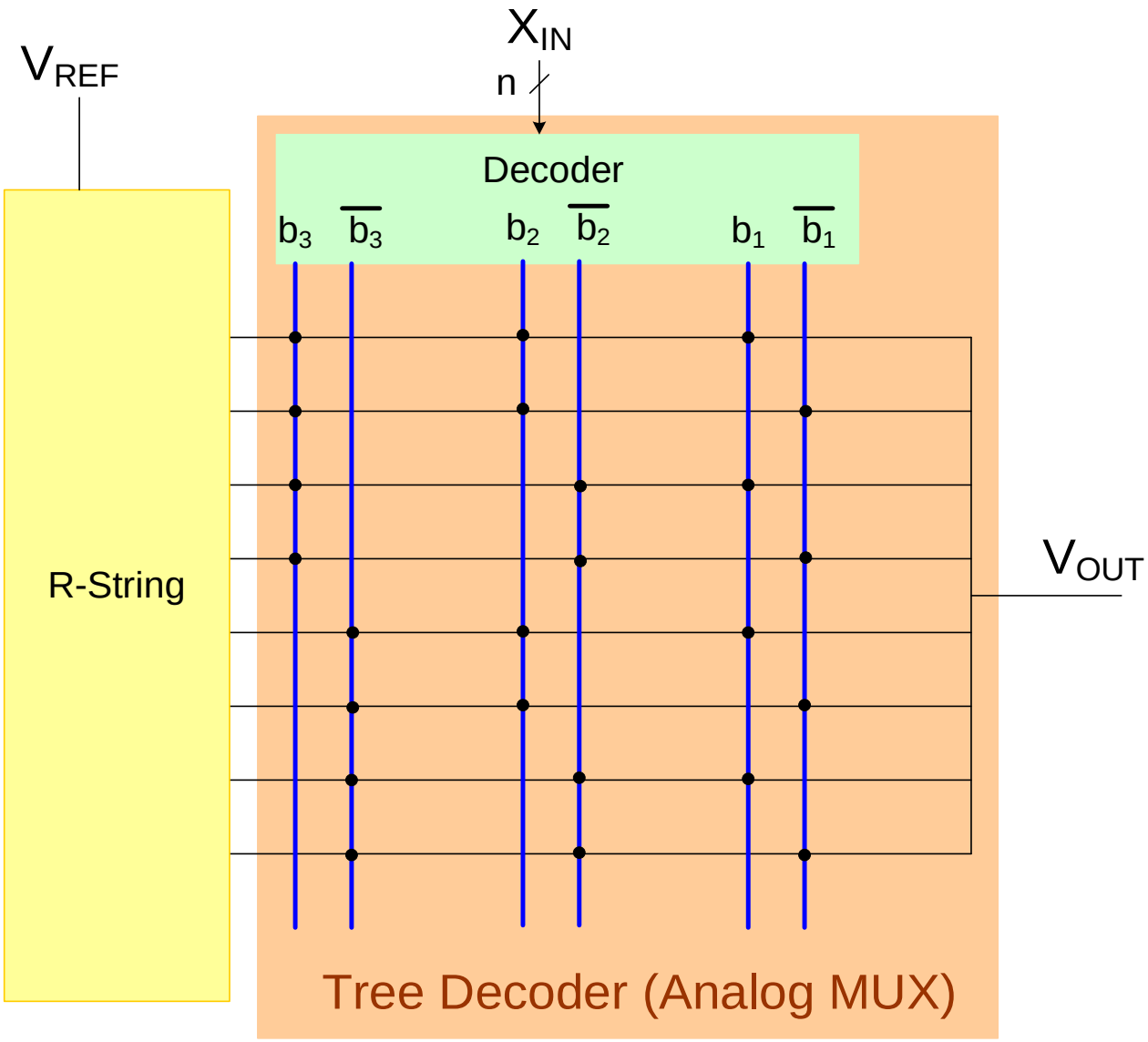
Routing of the 2^n switch signals can become very long and consume lots of area



Basic R-String DAC



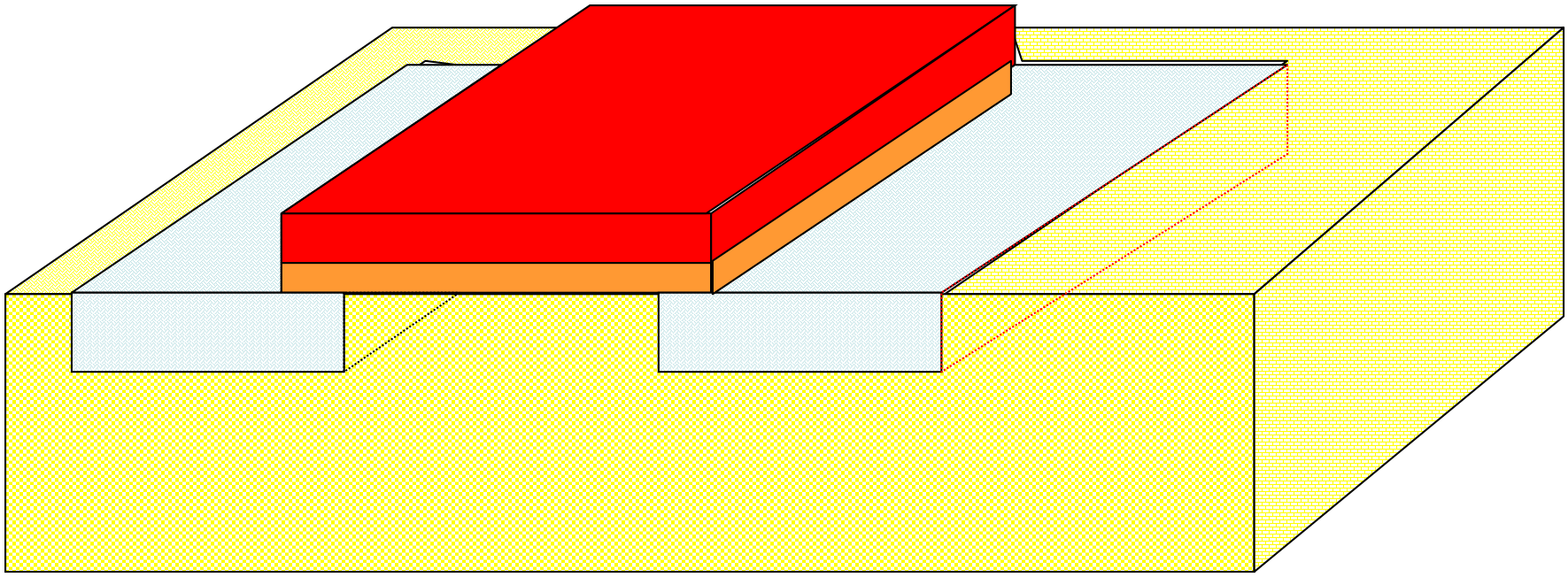
R-String DAC


V_{REF}
X_{IN}
n
Decoder
b_3
$\overline{b_3}$
b_2
$\overline{b_2}$
b_1
$\overline{b_1}$
R-String
V_{OUT}
Tree Decoder (Analog MUX)

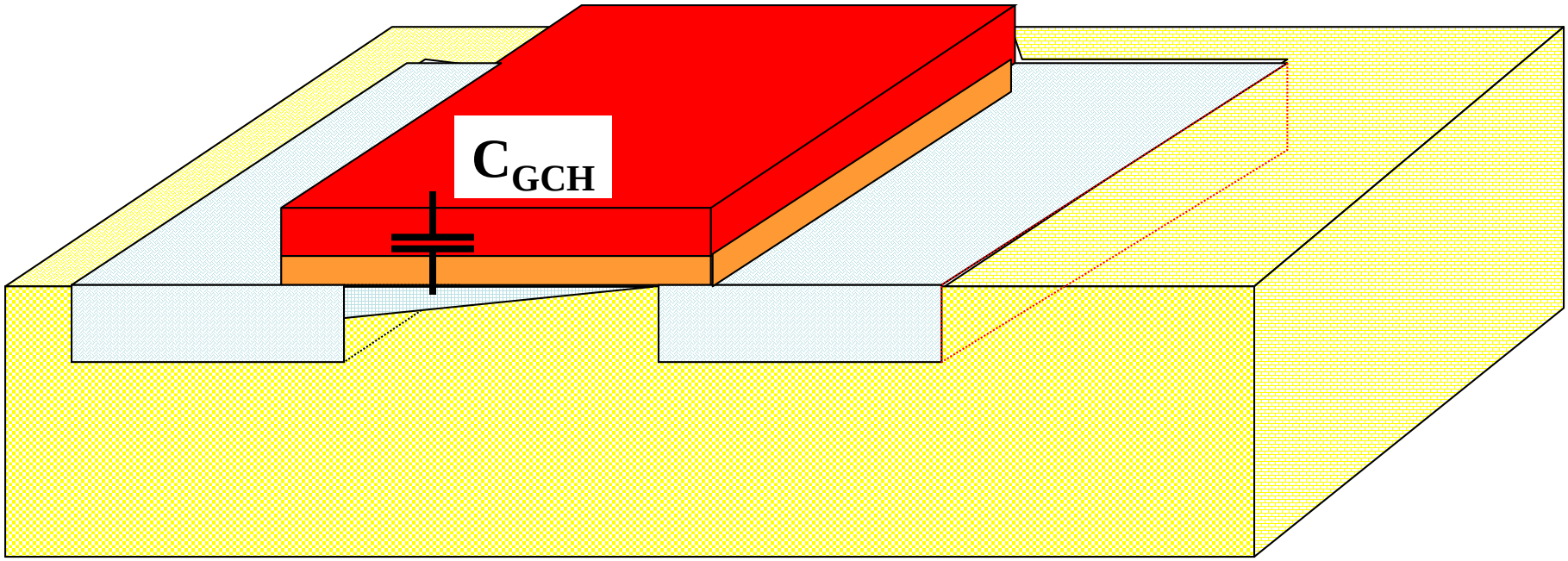
(Review from: EE 330 Lecture 36 Fall 2019)

Parasitic Capacitors in MOSFET

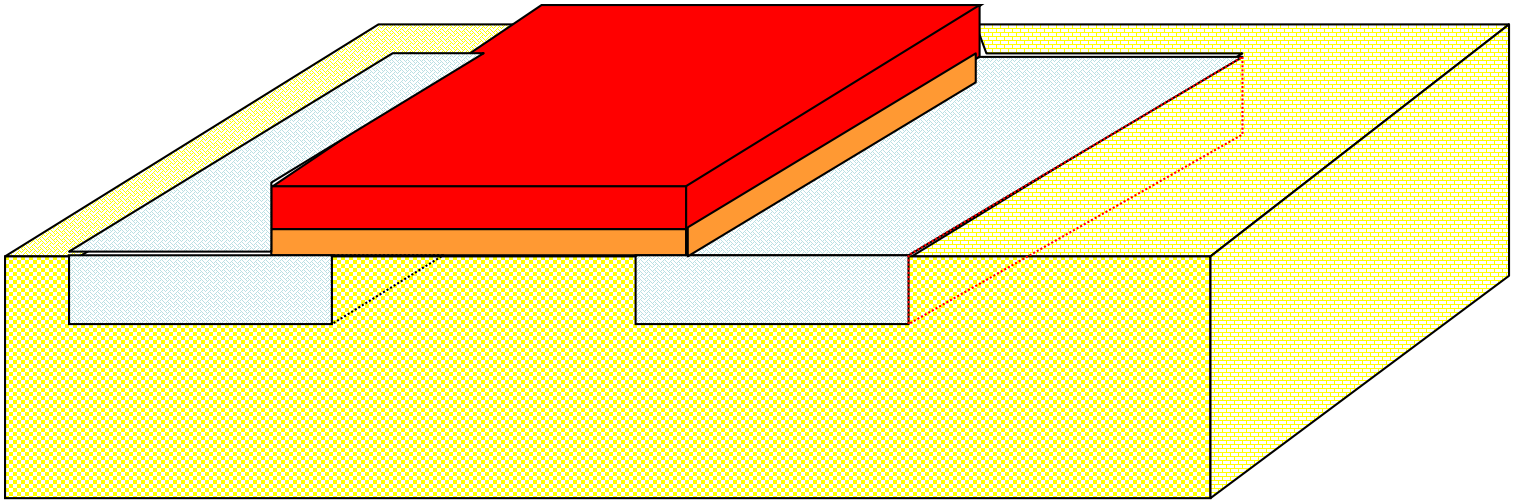
(will initially consider two: Gate-channel and diffusion)



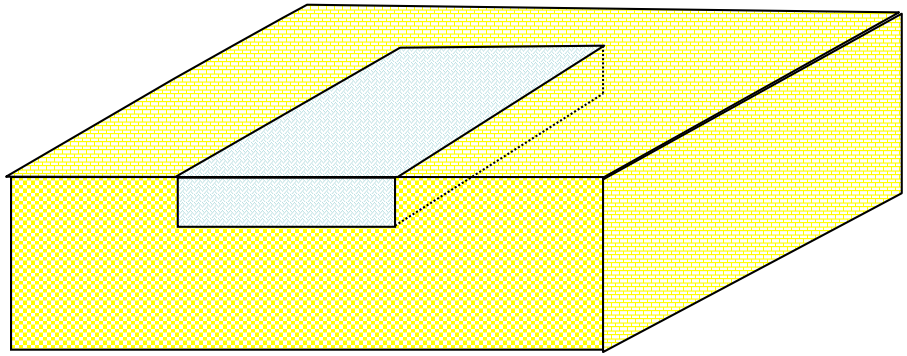
Parasitic Capacitors in MOSFET



Parasitic Capacitors in MOSFET

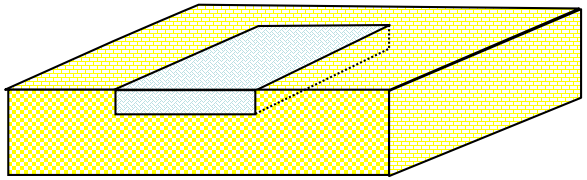


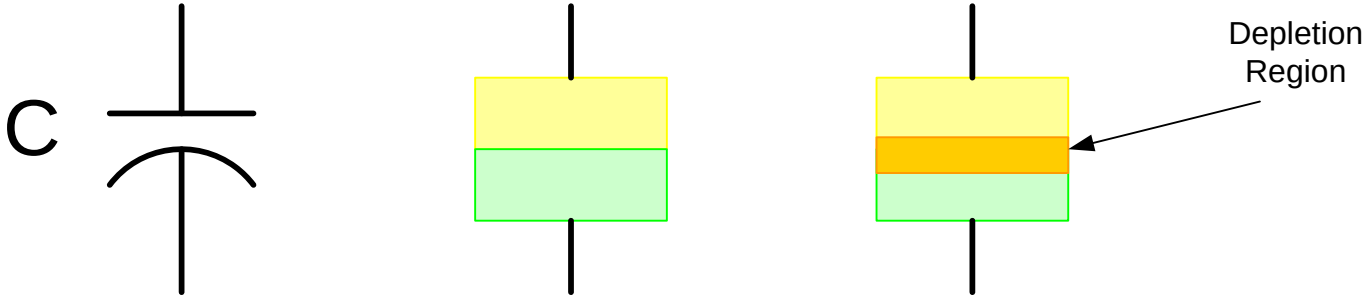
Recall that pn junctions have a depletion region!



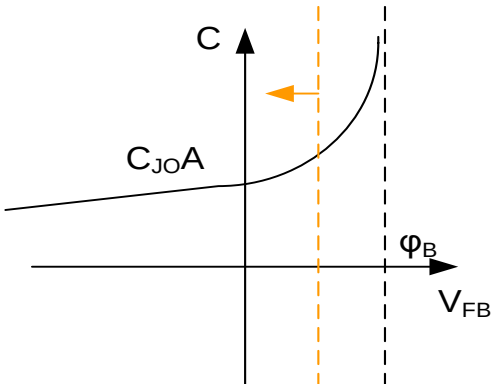
Parasitic Capacitors in MOSFET

pn junction capacitance





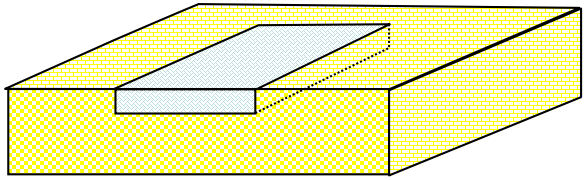
For $V_{FB}<\varphi_B/2$



$$C = \frac{C_{J0} A}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

Parasitic Capacitors in MOSFET

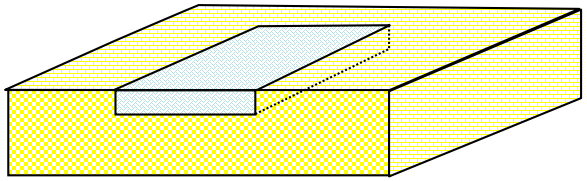
pn junction capacitance

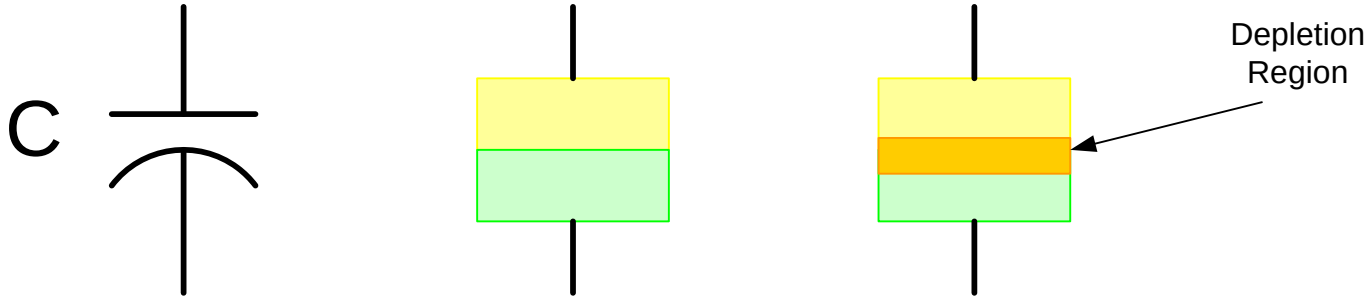


The bottom and the sidewall:

Parasitic Capacitors in MOSFET

pn junction capacitance





For a pn junction capacitor

$$C_J = C_{BOT} A + C_{SW} P$$

$$C_{BOT} = \frac{C_{BOT} A}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

$$C_{SW} = \frac{C_{SW} P}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

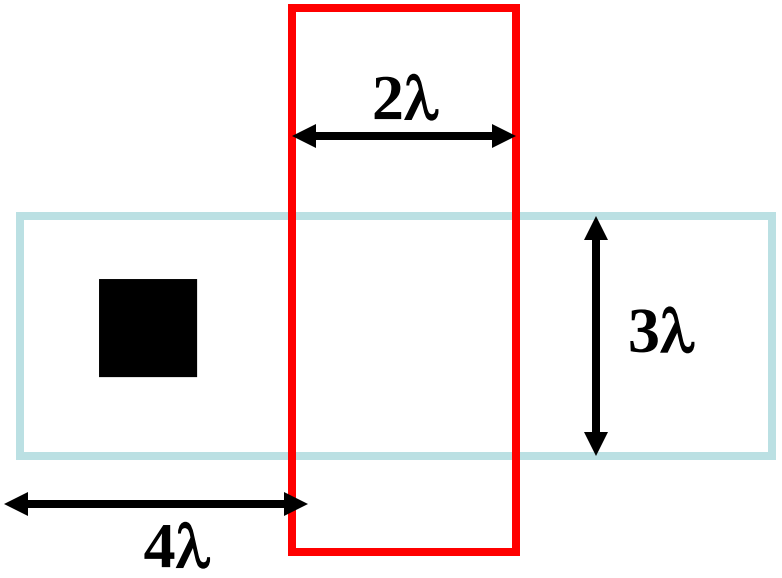
Question

- Are the parasitic capacitors relevant?

Observation

- Parasitic Capacitors are Small

Consider a minimum-sized transistor



Process Parameters from AMI 0.5u Process

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_	HR POLY2	MTL1	MTL2	UNITS
Sheet Resistance	81.5	101.9	21.6	1120	41	0.09	0.09	ohms/sq
Contact Resistance	64.6	141.9	15.8		26.8		0.8	ohms
Gate Oxide Thickness	140							angstrom

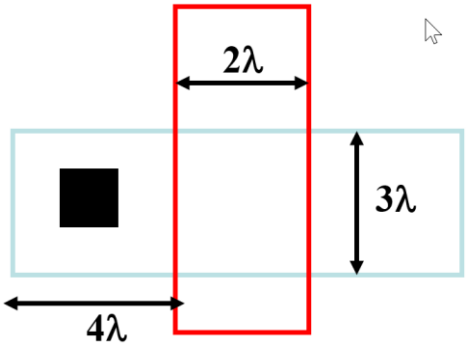
PROCESS PARAMETERS	MTL 3	N\PLY	N WELL					
Sheet Resistance	0.06	822	812					ohms/sq
Contact Resistance	0.65							ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	424	731	87		32	16	10	39	aF/um^2
Area (N+active)			2473		36	16	12		aF/um^2
Area (P+active)			2382						aF/um^2
Area (poly)				969	56	15	10		aF/um^2
Area (poly2)					50				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							39		aF/um^2
Fringe (substrate)	315	247			72	58	38		aF/um
Fringe (poly)					57	39	28		aF/um
Fringe (metal1)						48	34		aF/um
Fringe (metal2)							55		aF/um
Overlap (N+active)			195						aF/um
Overlap (P+active)			239						aF/um

λ=.35 microns

Size of Capacitances



Gate-Channel Capacitance = $6\lambda^2$ x 2.47fF/μ^2 = 1.82fF

Source Diffusion-Substrate Capacitance =
$12\lambda^2$ x .424fF/μ^2 + 14λ x .315fF/μ =
.624fF + 1.54fF =2.16fF

Note Sidewall Capacitance larger than Bottom Capacitance

Are these negligible?

Are these negligible?

These small capacitors play the dominant role in the speed limitations of most digital circuits

These small capacitors play a major role in the performance of many linear circuits

It is essential that these capacitors (parasitic capacitors) be considered and managed when designing most integrated circuits today!

Types of Capacitors

1. Fixed Capacitors
   a. Fixed Geometry
   b. Junction

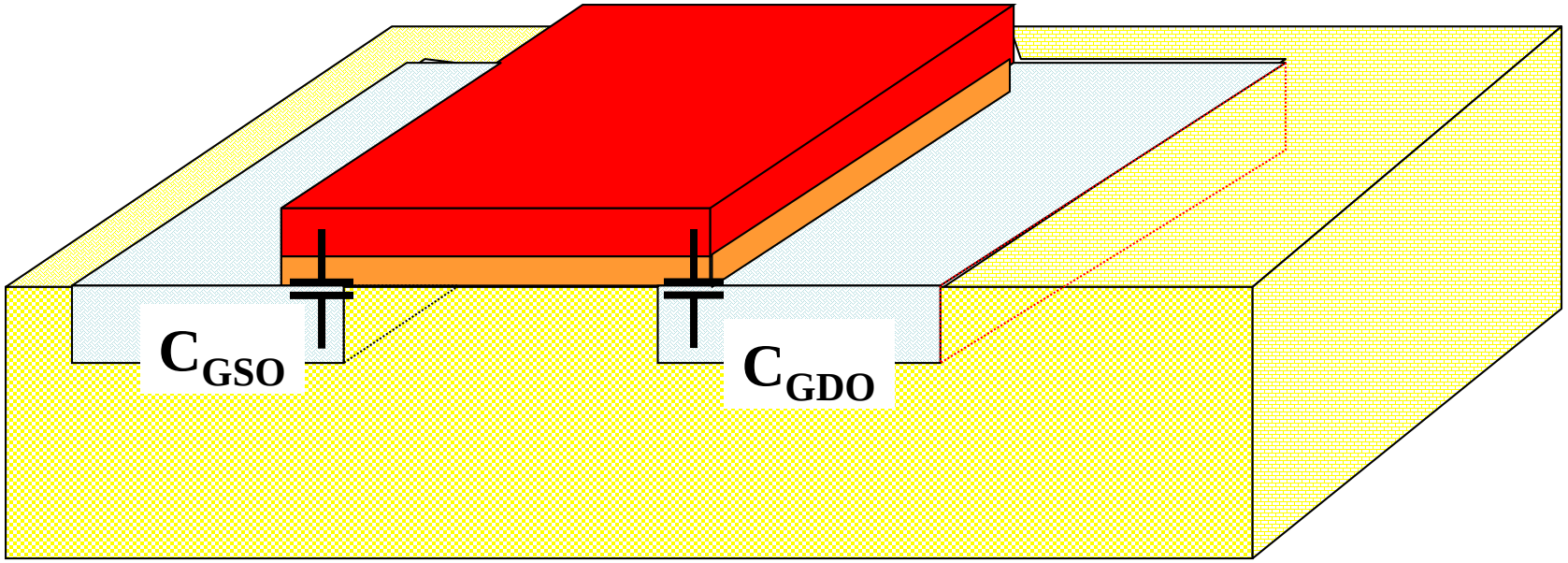
2. Operating Region Dependent
   a. Fixed Geometry
   b. Junction

Parasitic Capacitors in MOSFET

Fixed Capacitors

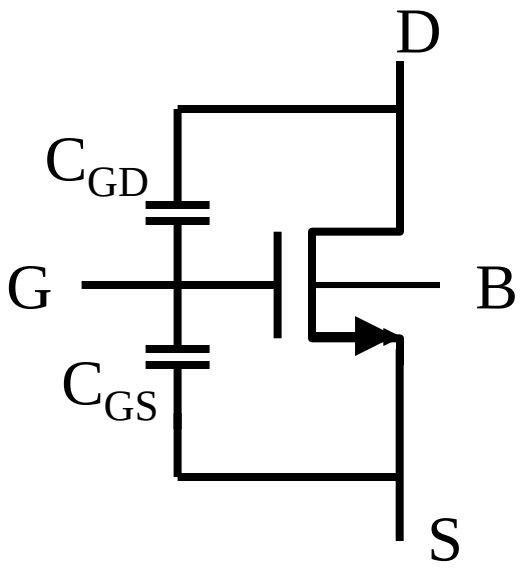
Parasitic Capacitors in MOSFET

Fixed Capacitors



Overlap Capacitors: C_{GDO}, C_{GSO}

Parasitic Capacitance Summary

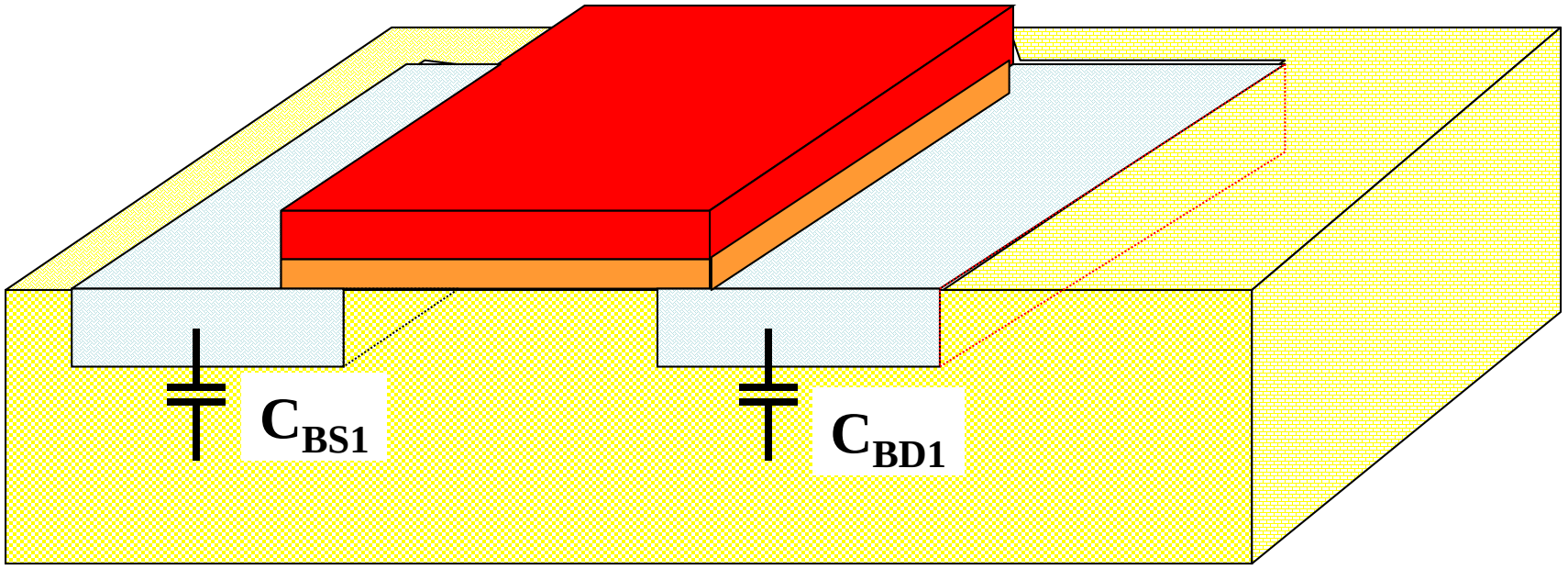


	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{GD}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$

L_D is a model parameter

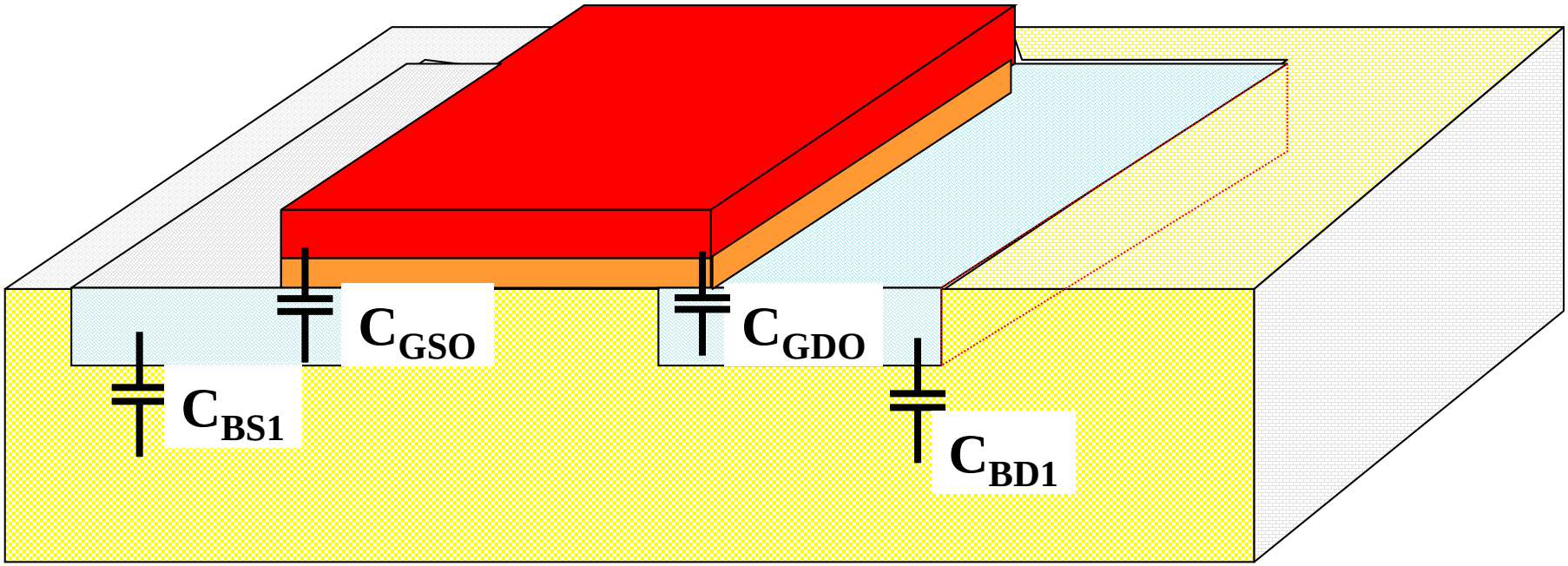
Parasitic Capacitors in MOSFET

Fixed Capacitors



Junction Capacitors: C_{BS1}, C_{BD1}

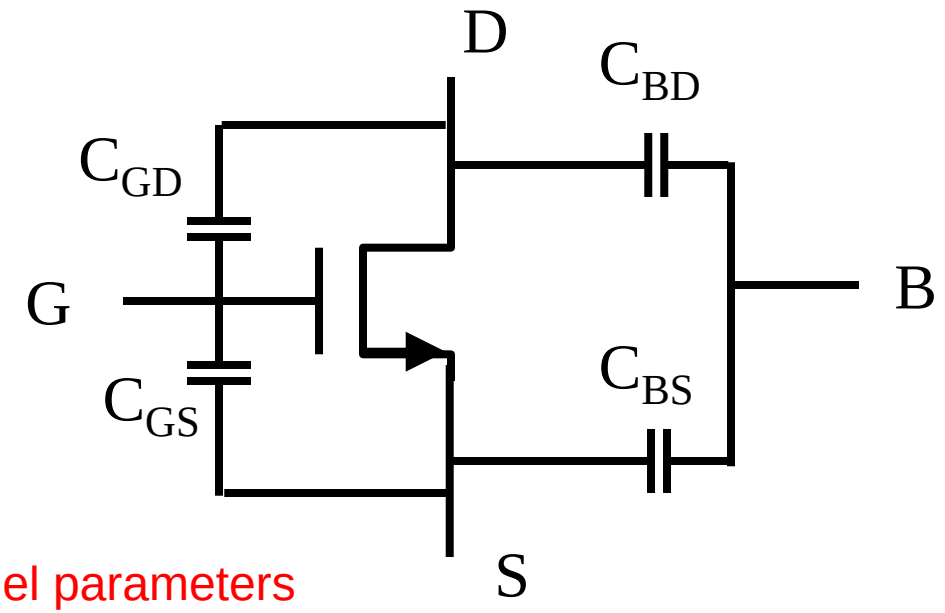
Parasitic Capacitors in MOSFET
Fixed Capacitors



Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Fixed Parasitic Capacitance Summary



C_{BOT} and C_{SW} are model parameters

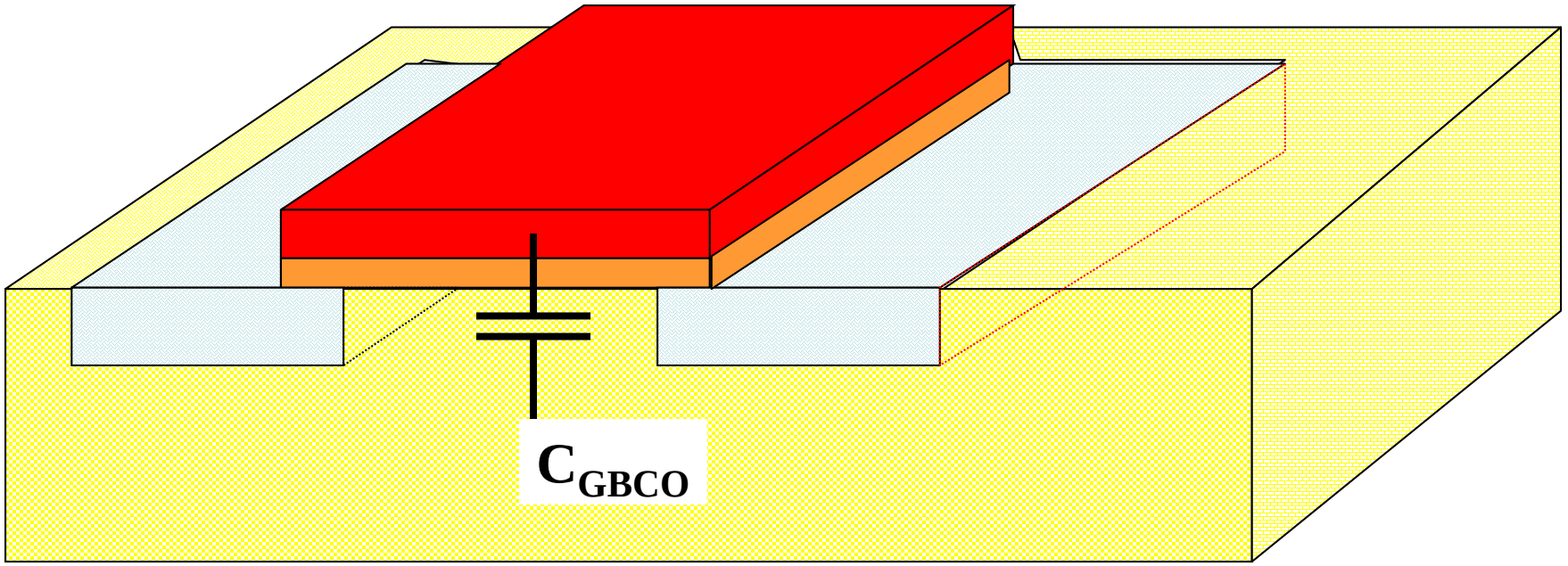
	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{GD}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{BG}			
C_{BS}	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$
C_{BD}	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$

Parasitic Capacitors in MOSFET

Operation Region Dependent

Parasitic Capacitors in MOSFET

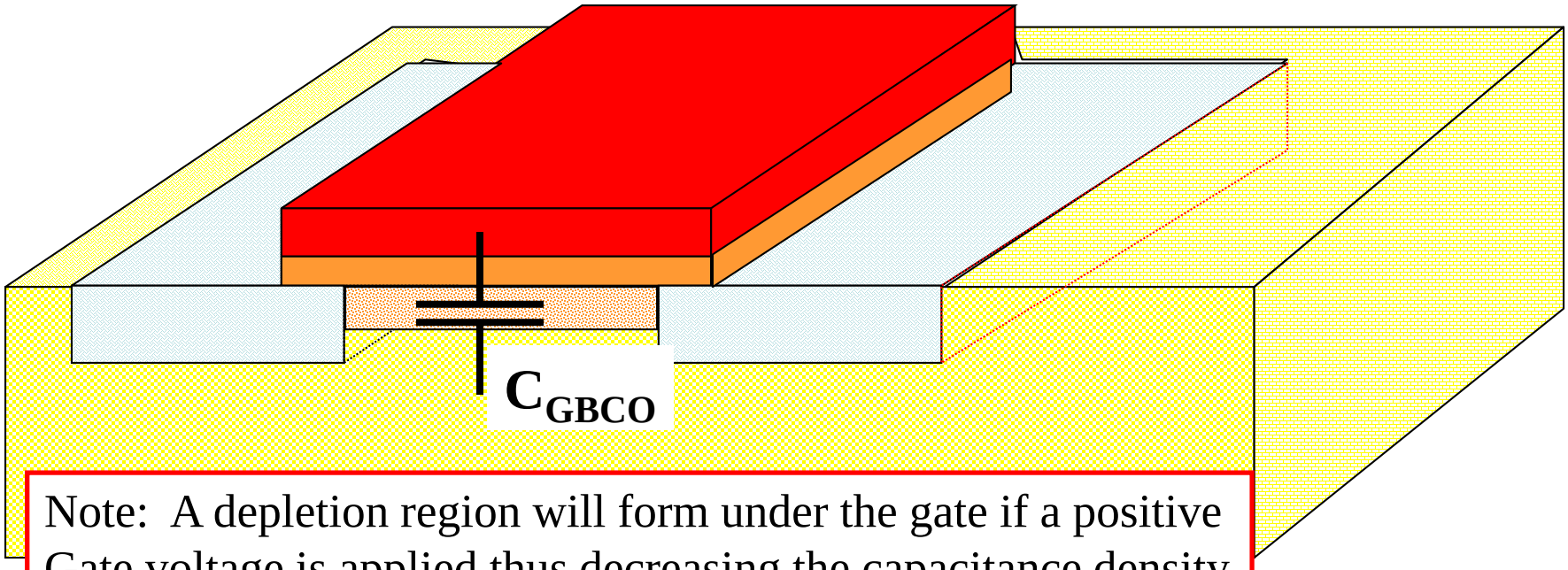
Operation Region Dependent -- Cutoff



Cutoff Capacitor: C_{GBCO}

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Cutoff

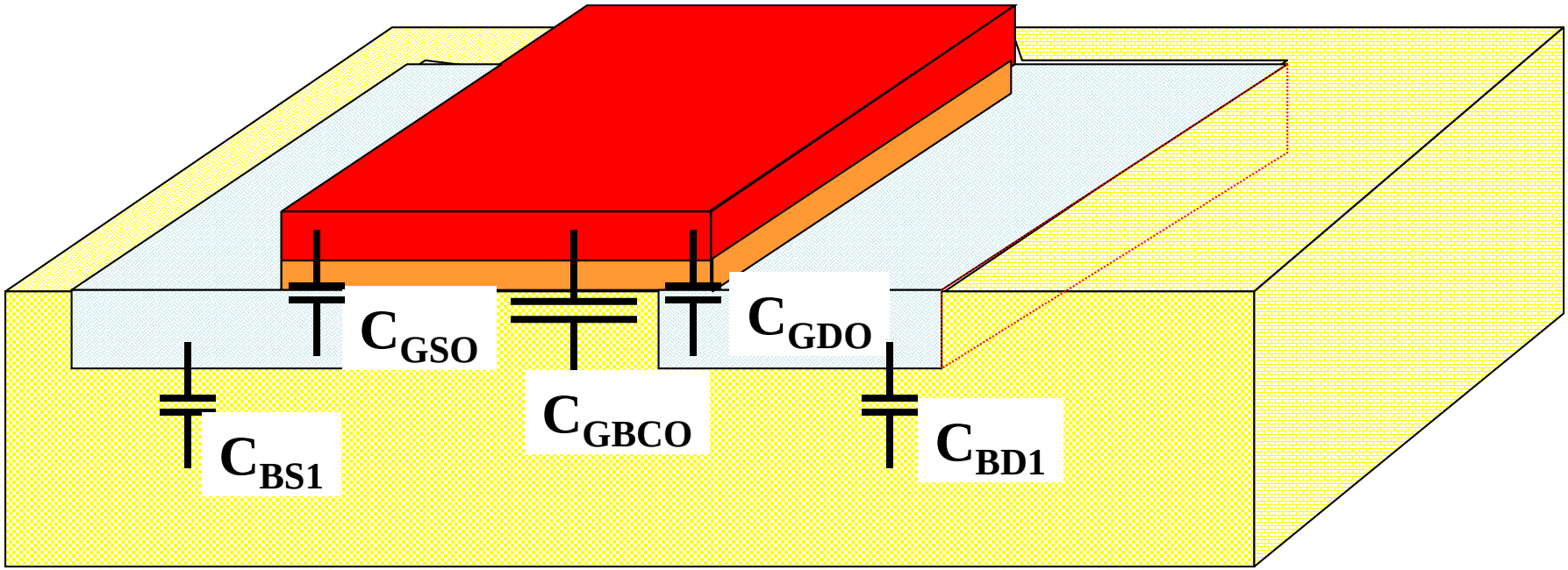


Note: A depletion region will form under the gate if a positive Gate voltage is applied thus decreasing the capacitance density

Cutoff Capacitor: C_{GBCO}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed -- Cutoff

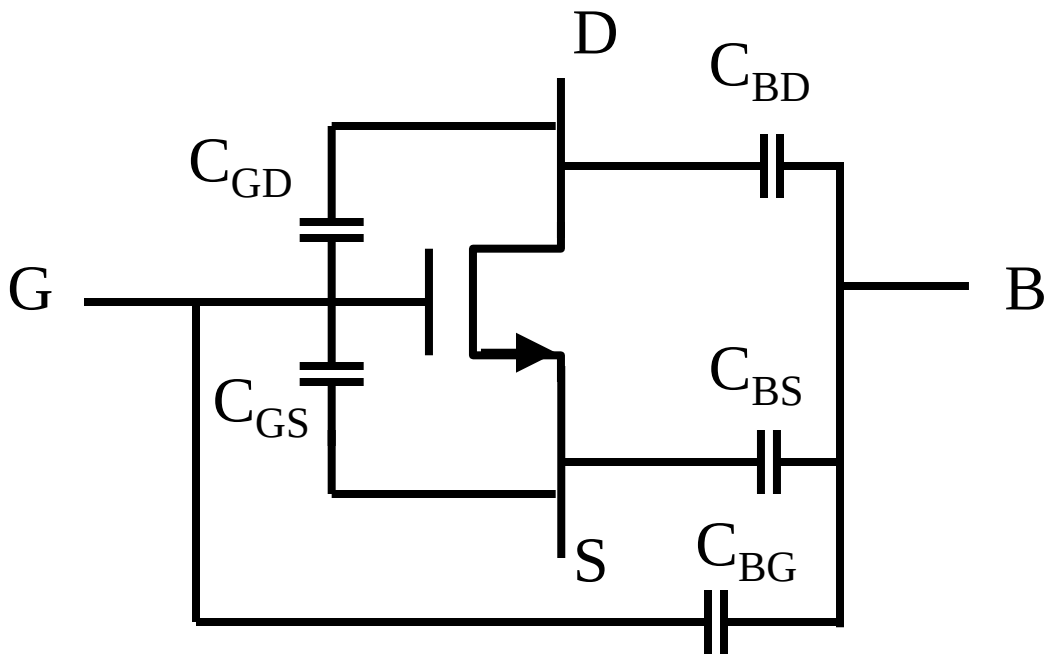


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Cutoff Capacitor: C_{GBCO}

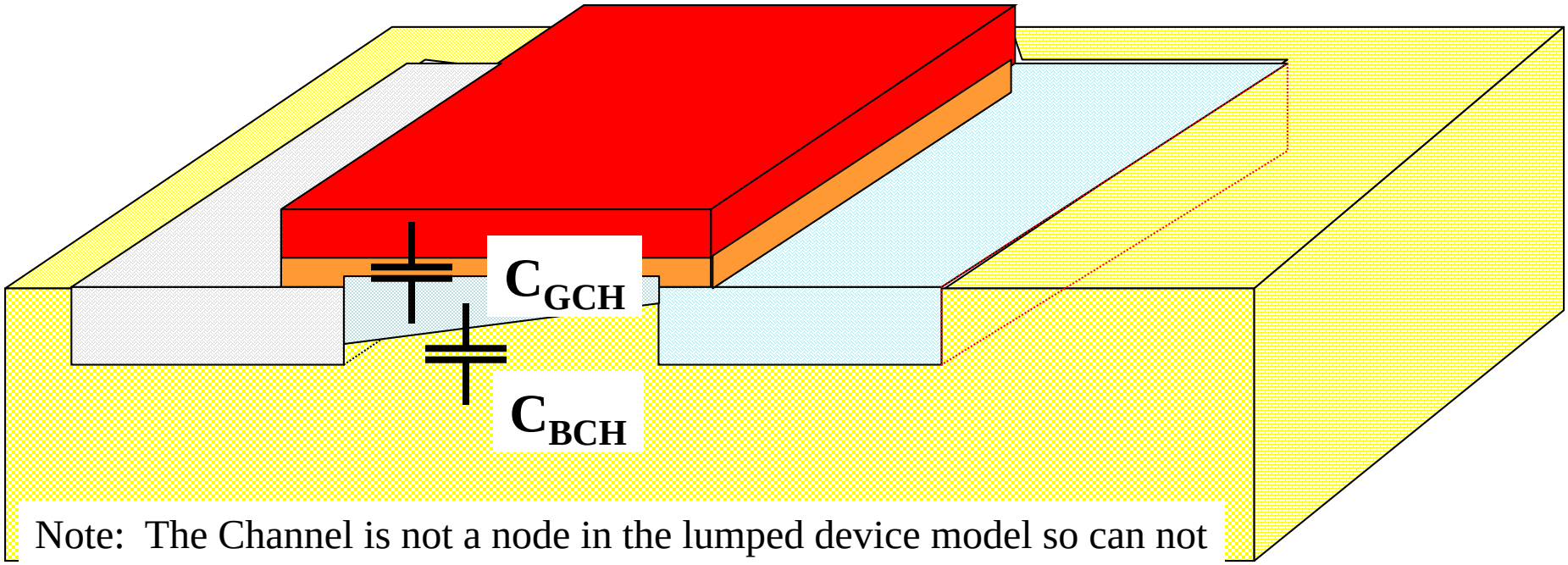
Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{GD}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{BG}	CoxWL (or less)		
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Ohmic



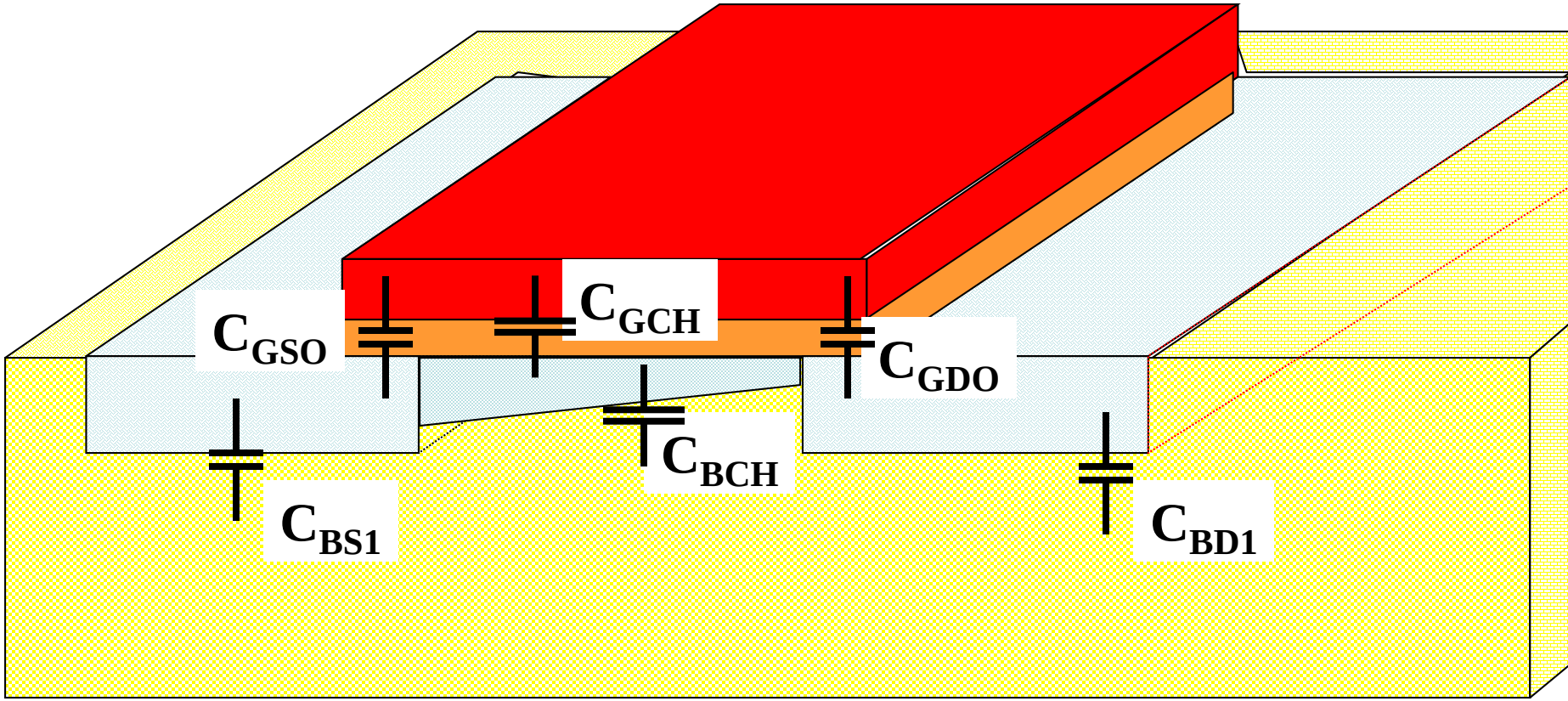
Note: The Channel is not a node in the lumped device model so can not directly include this distributed capacitance in existing models

Note: The distributed channel capacitance is usually lumped and split evenly between the source and drain nodes

Ohmic Capacitor: C_{GCH}, C_{BCH}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed -- Ohmic

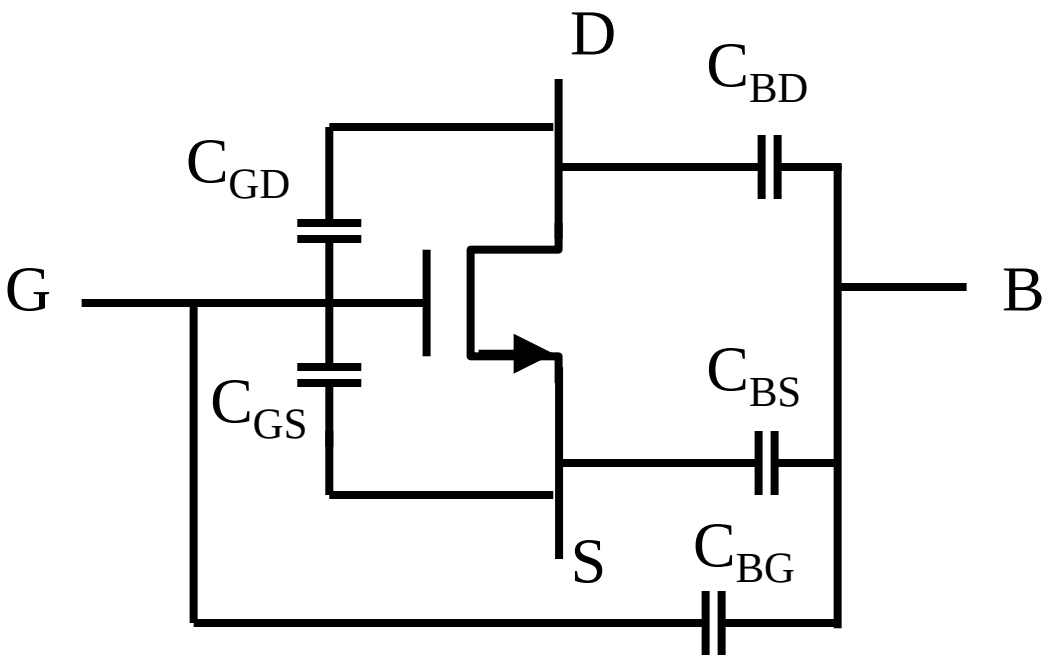


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Ohmic Capacitor: C_{GCH}, C_{BCH}

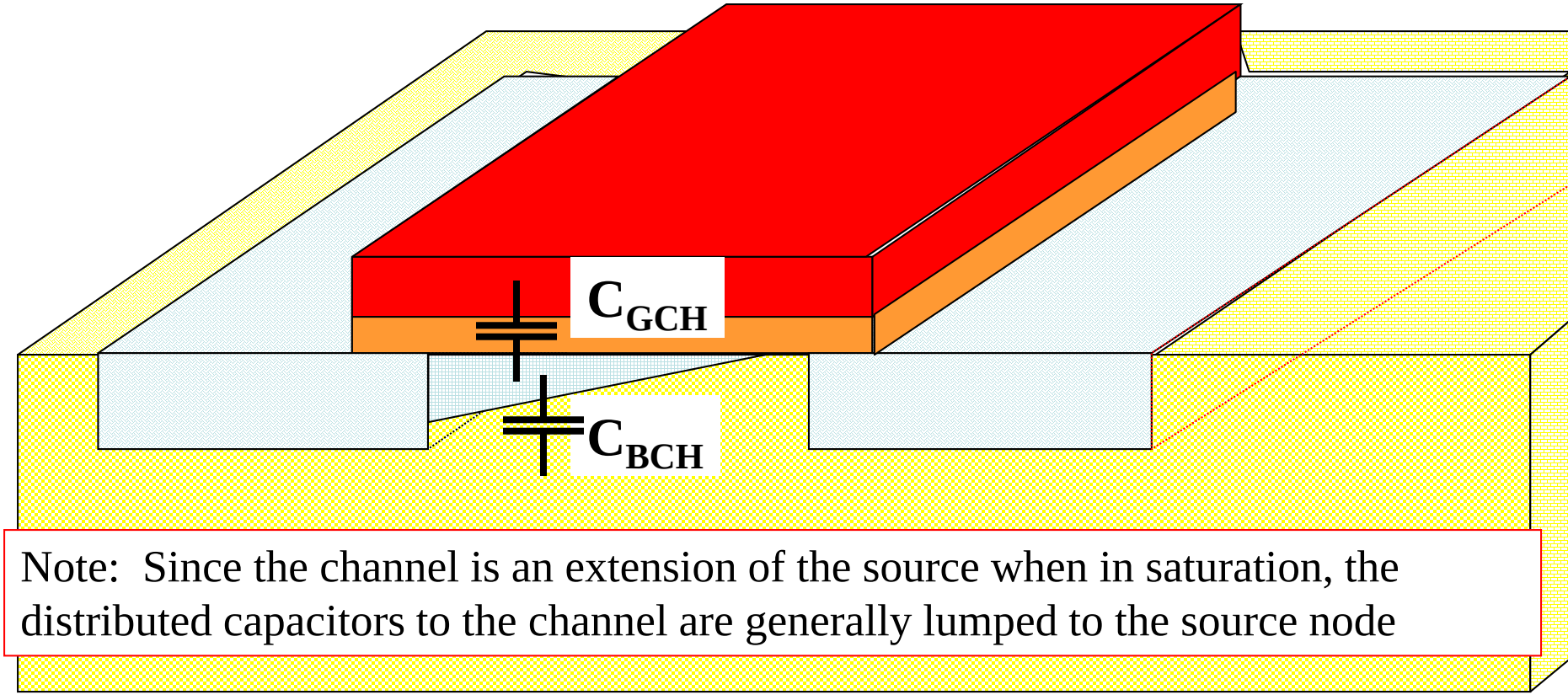
Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{GD}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{BG}	CoxWL (or less)		
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Saturation

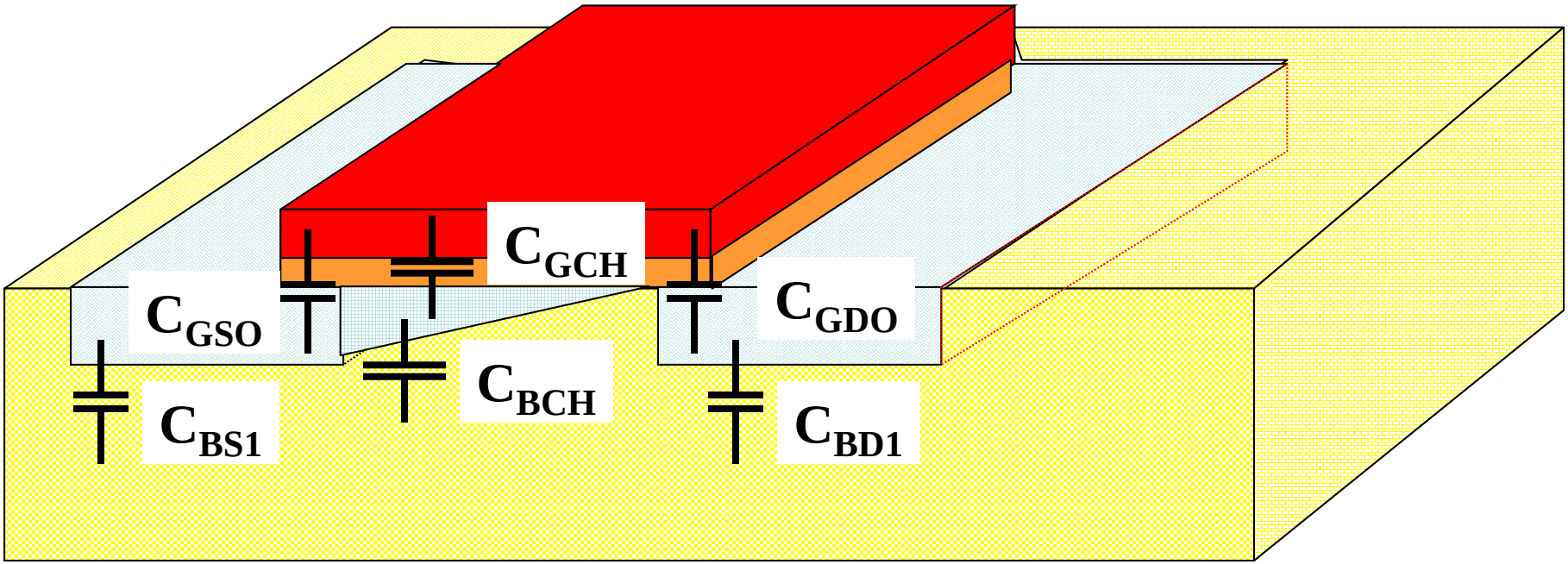


Note: Since the channel is an extension of the source when in saturation, the distributed capacitors to the channel are generally lumped to the source node

Saturation Capacitors: C_{GCH}, C_{BCH}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed --Saturation

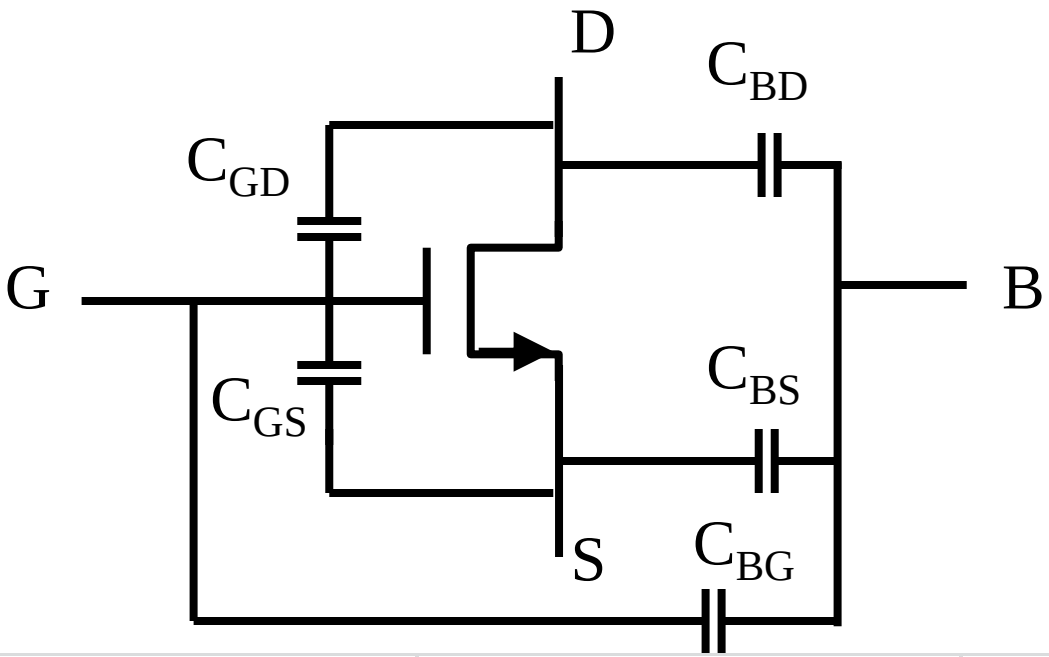


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

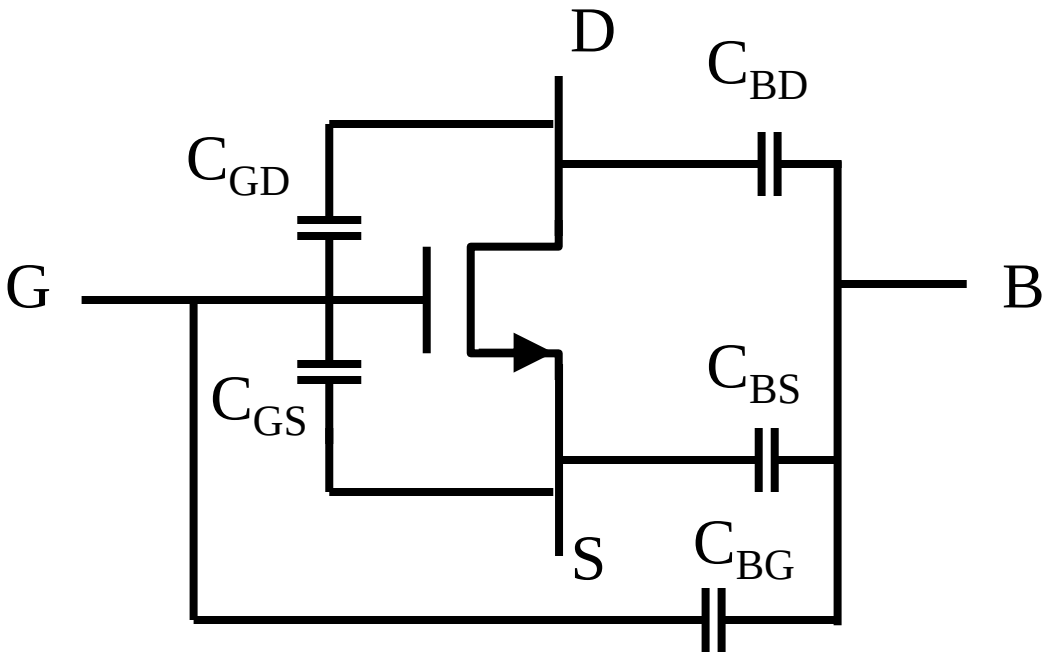
Saturation Capacitors: C_{GCH}, C_{BCH}

Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D + 0.5C_{OX}WL$	$CoxWL_D+(2/3)C_{OX}WL$
C_{GD}	$CoxWL_D$	$CoxWL_D + 0.5C_{OX}WL$	$CoxWL_D$
C_{BG}	CoxWL (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S+(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

Parasitic Capacitance Summary

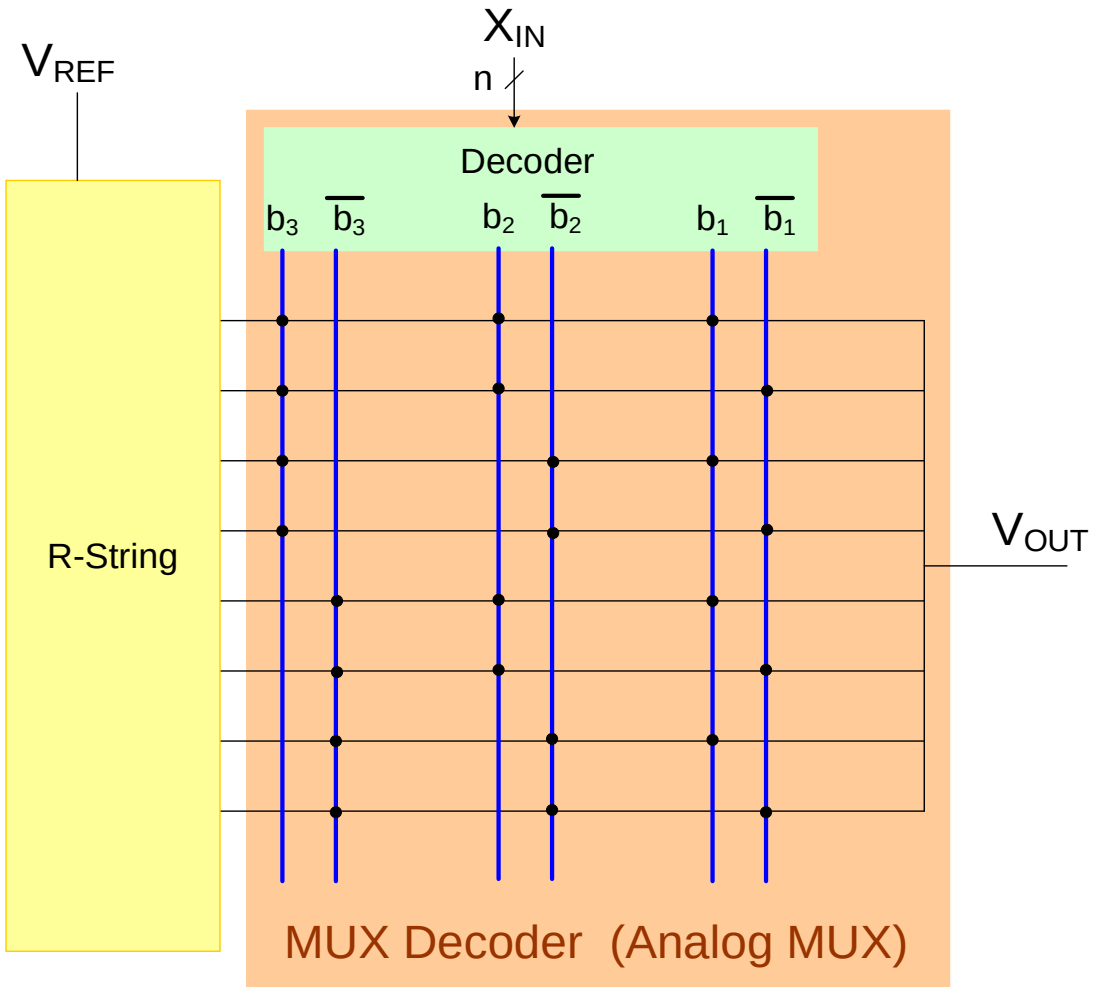


	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D + 0.5C_{OX}WL$	$CoxWL_D+(2/3)C_{OX}WL$
C_{GD}	$CoxWL_D$	$CoxWL_D + 0.5C_{OX}WL$	$CoxWL_D$
C_{BG}	CoxWL (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S +(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

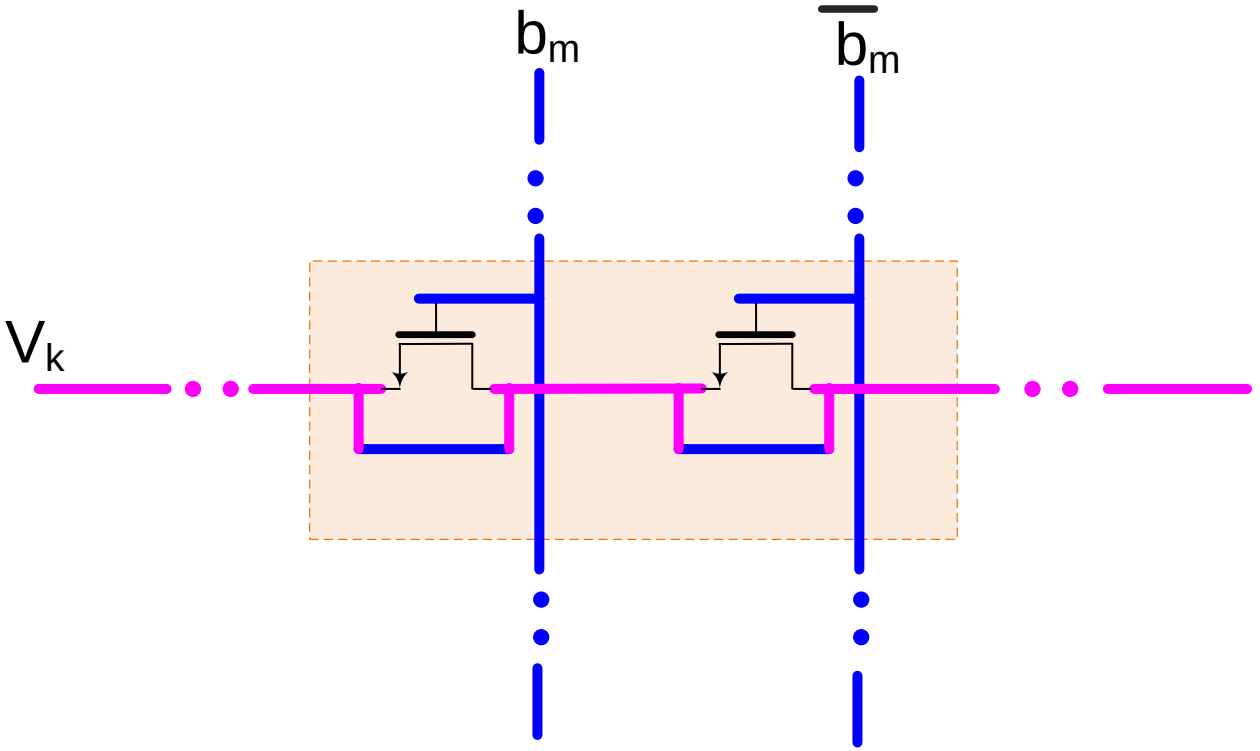
R-String DAC

Tree-Decoder Layout/Architecture

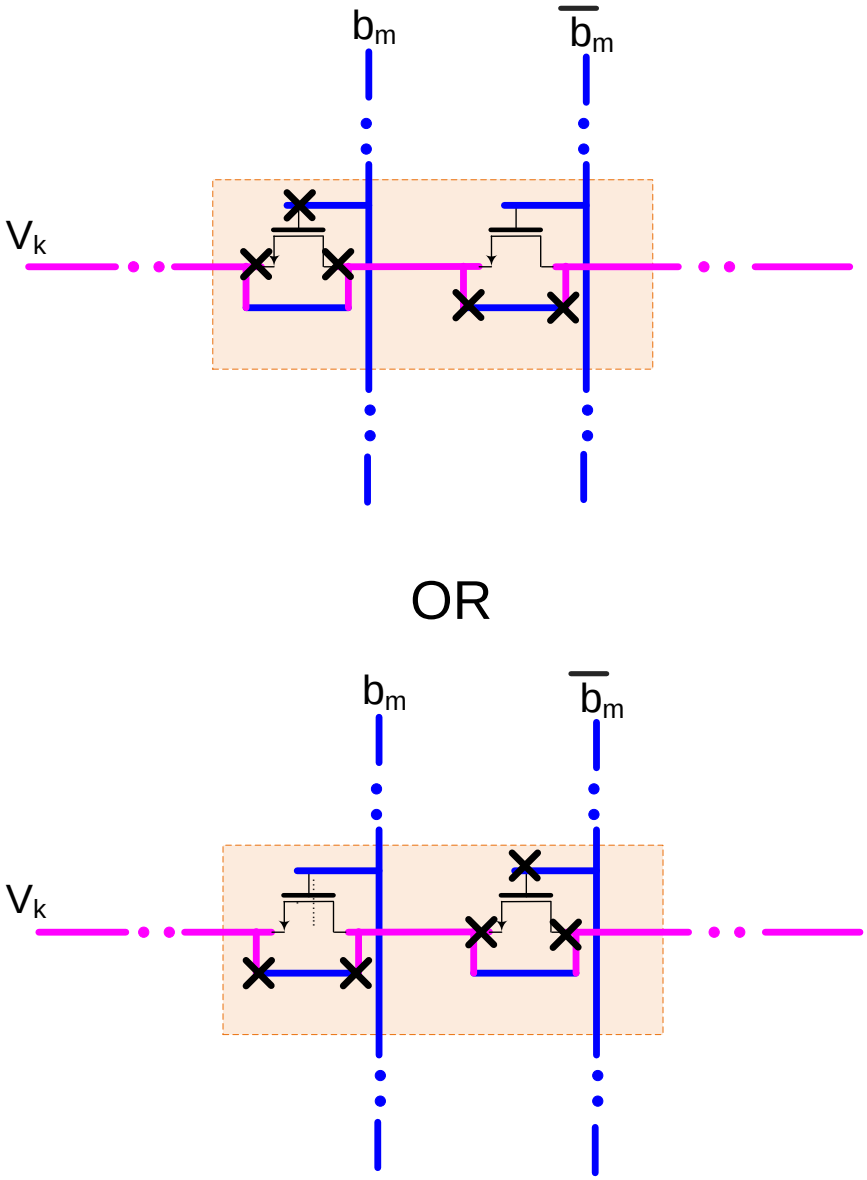
Each intersection is a reserved site for a switch



Uncontacted Row-Column Structure

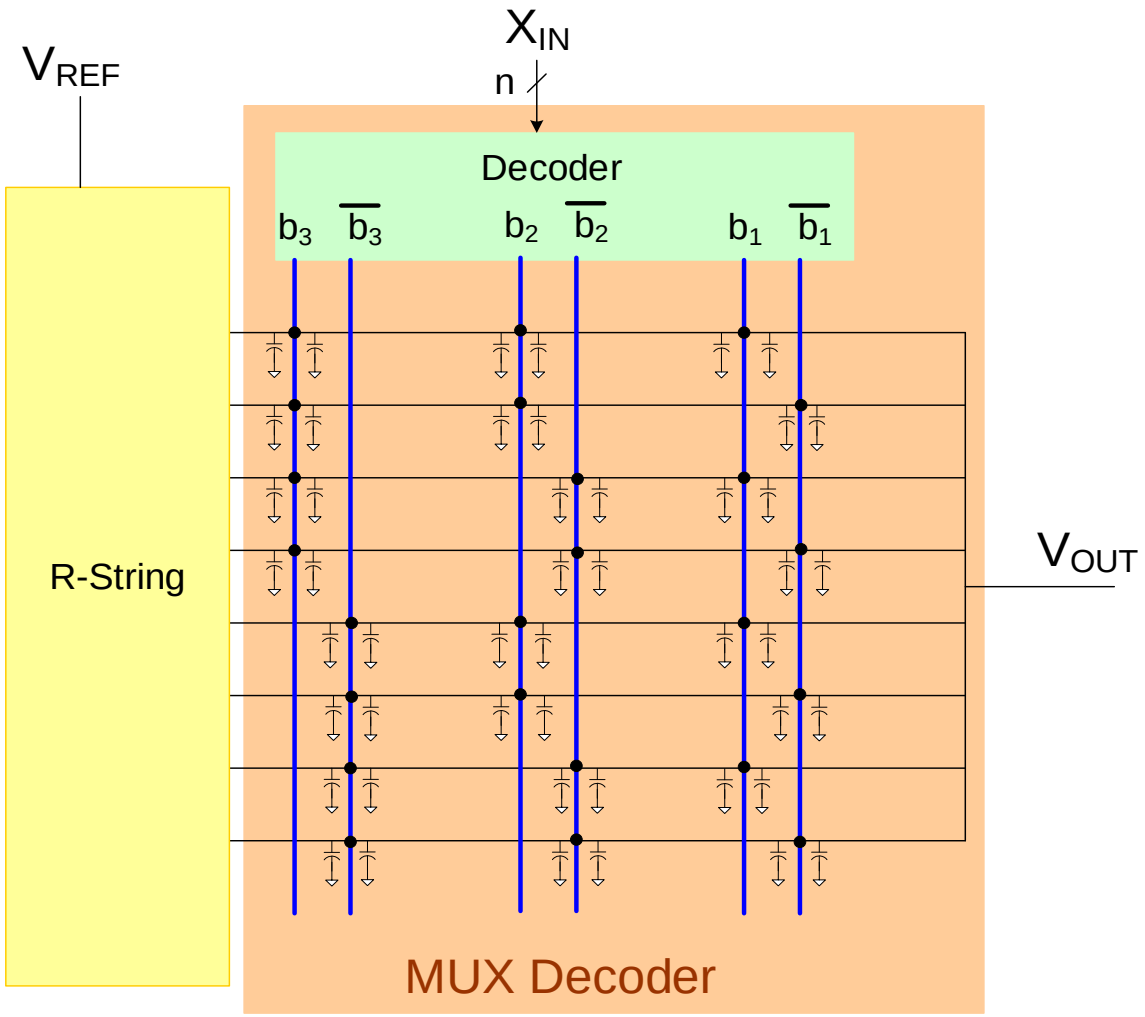


Row-Column Structure with Contacts Added



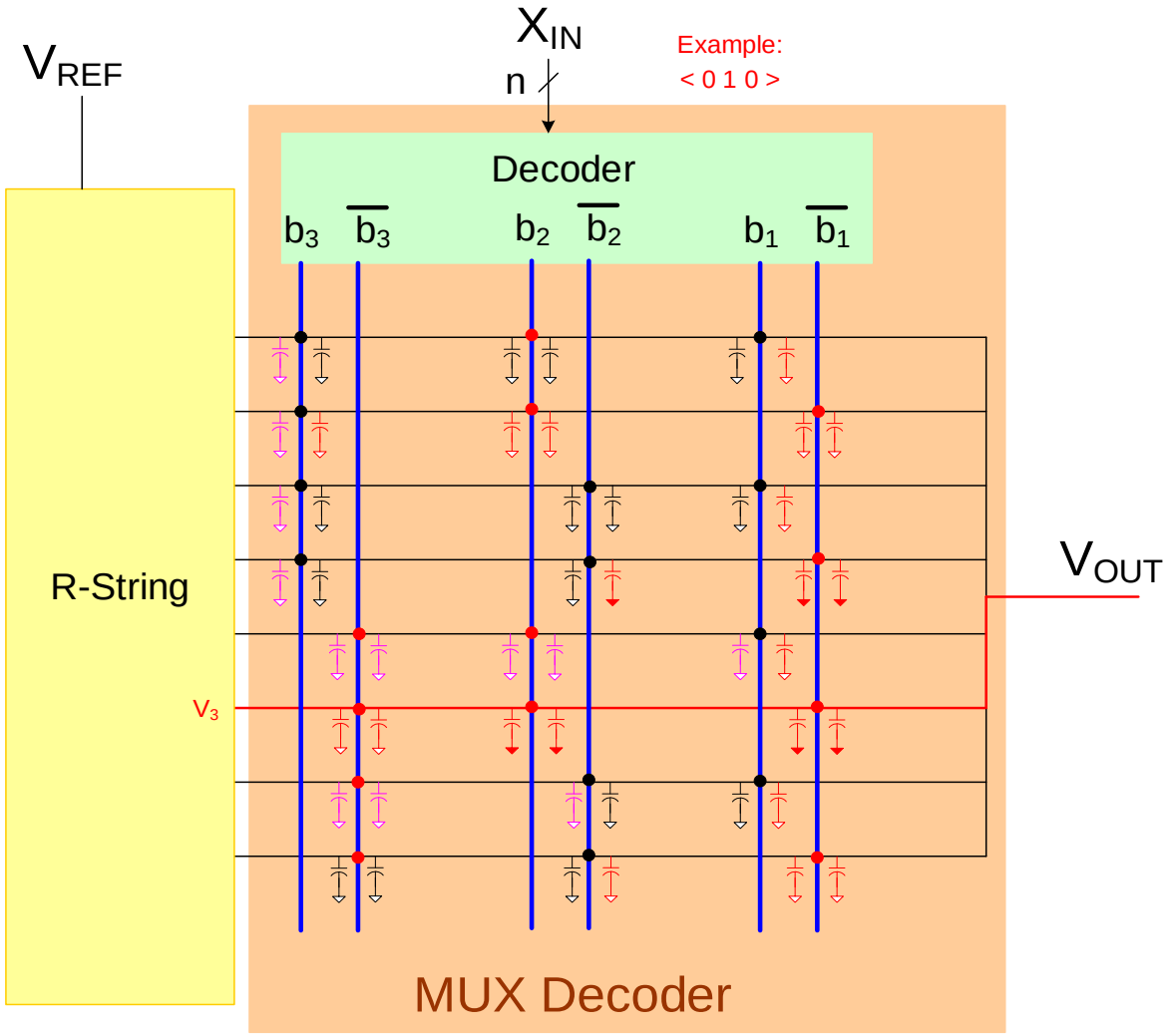
Programmed entirely with the contact mask

R-String DAC



Parasitic Capacitances in MUX Decoder

R-String DAC



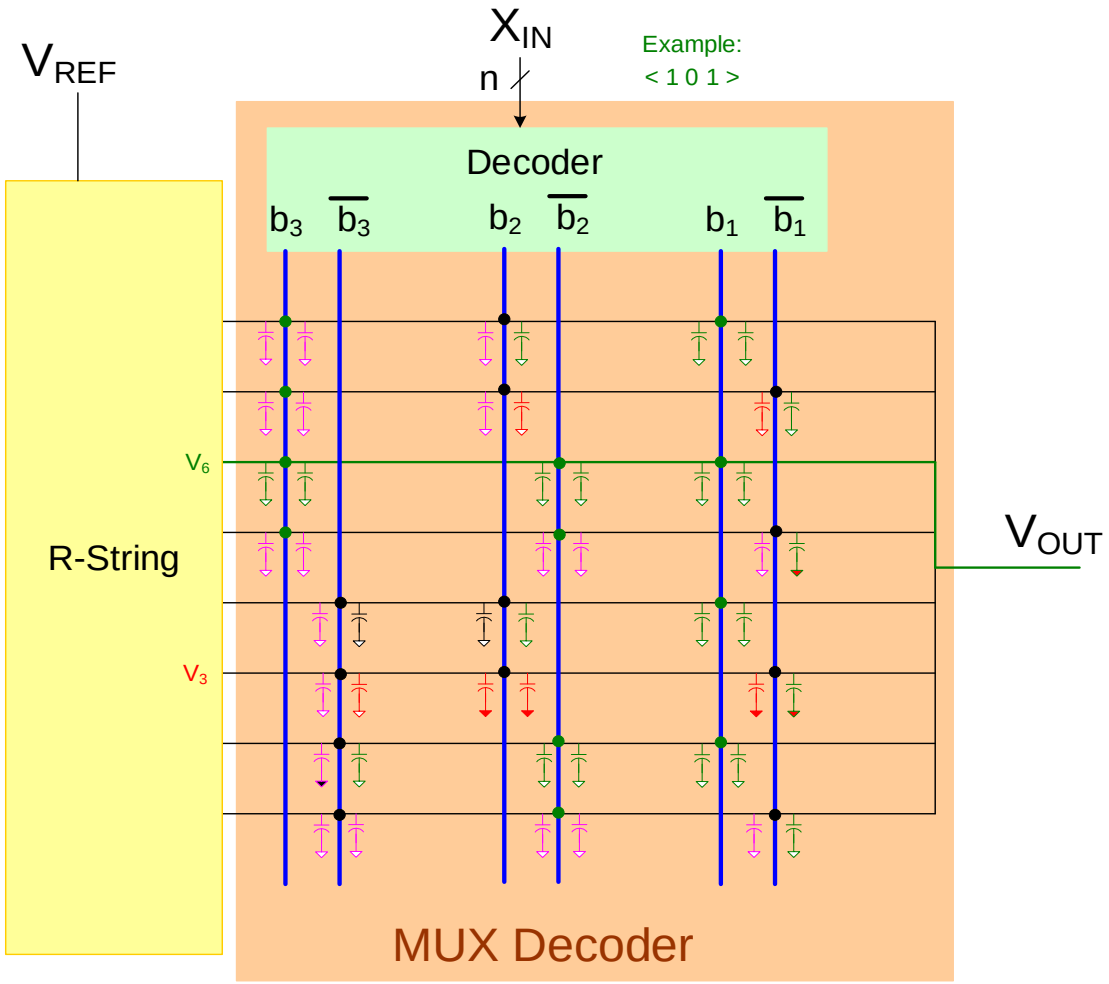
Previous-Code Dependent Settling

Assume all C's initially with 0V

Red denotes V_3, black denotes 0V, Purple some other voltage

R-String DAC

Transition from <010> to <101>



Previous-Code Dependent Settling

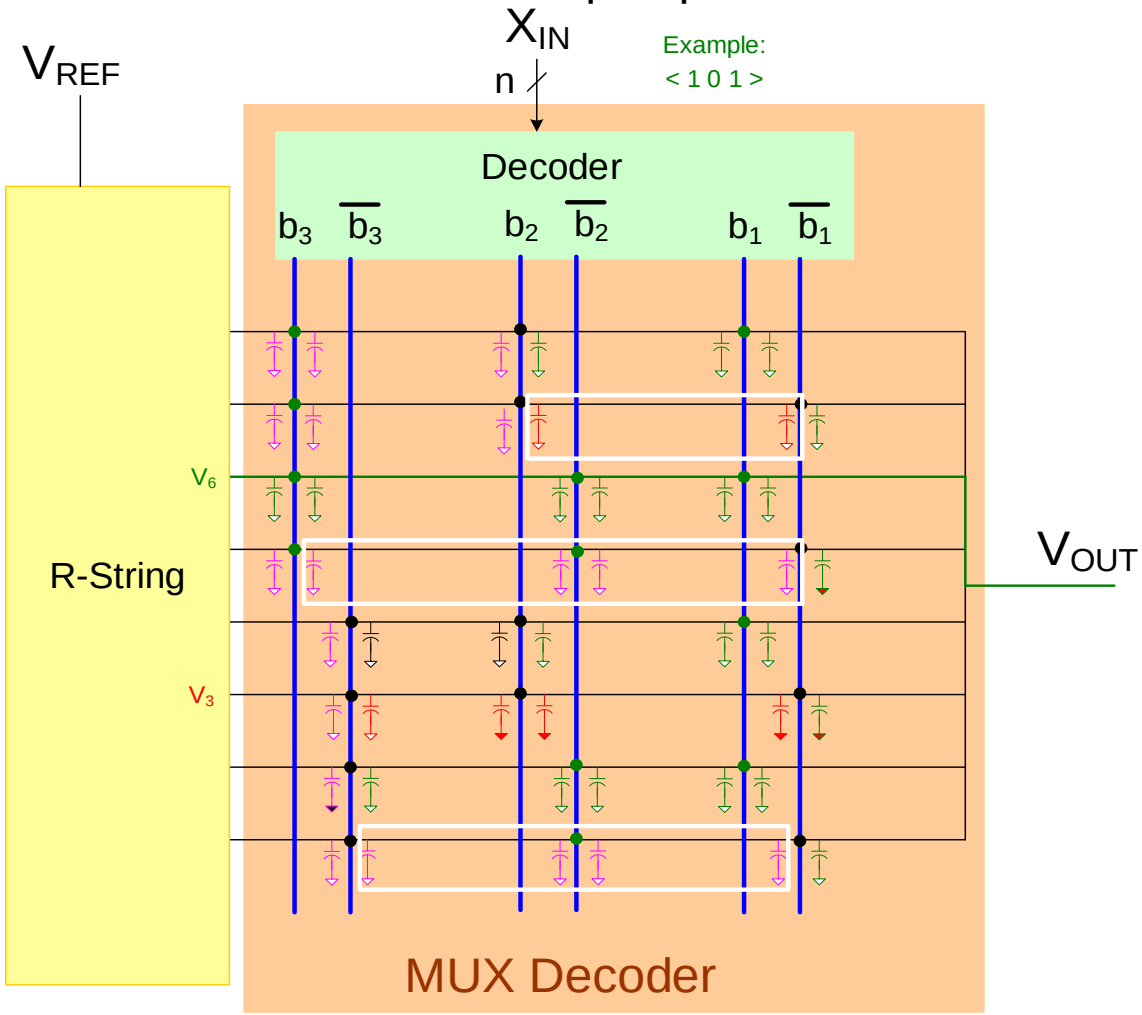
Assume all C's initially with 0V

Red denotes V_3, green denotes V_6, black denotes 0V, Purple some other voltage

R-String DAC

Transition from <010> to <101>

White boxes show capacitors dependent upon previous code <010>

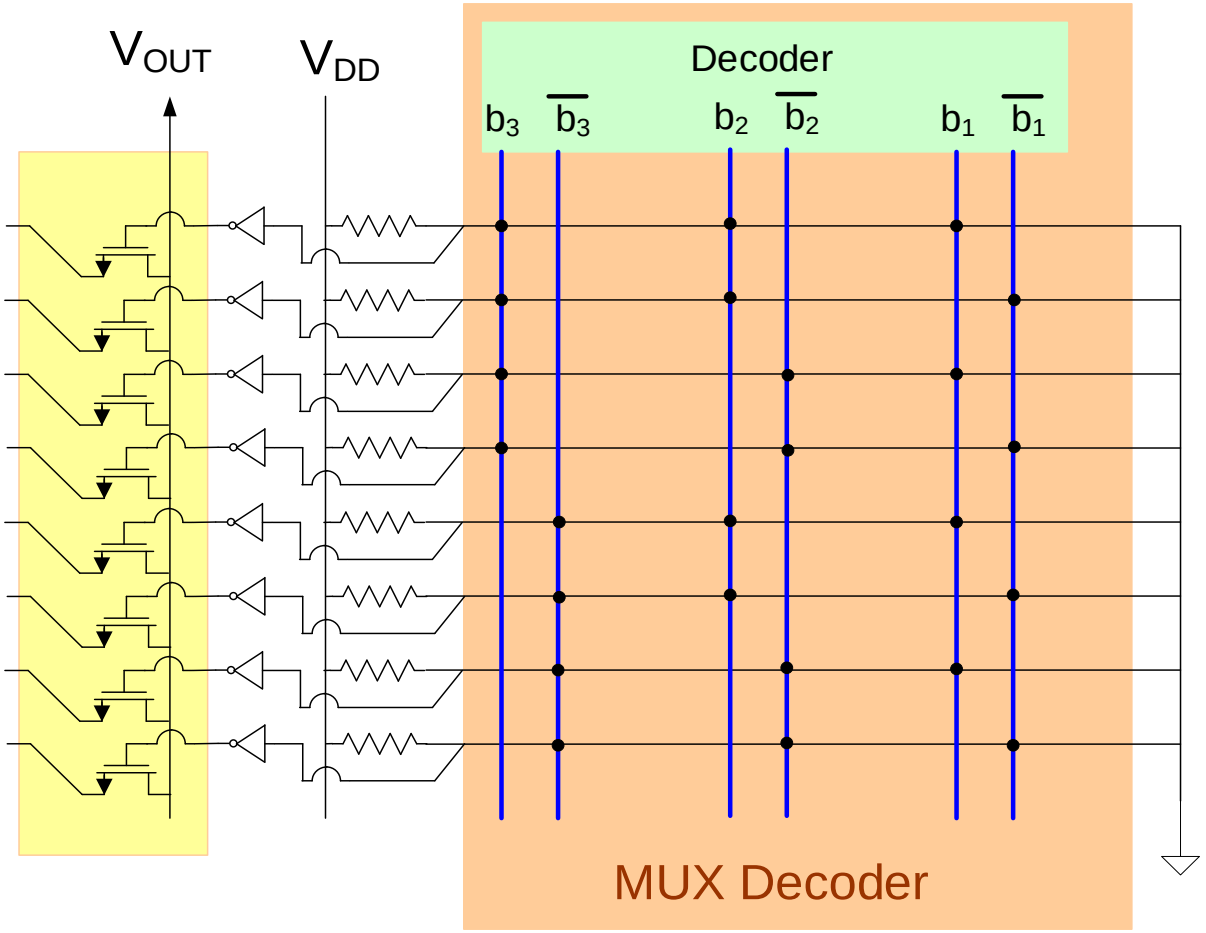


Previous-Code Dependent Settling

Assume all C's initially with 0V

Red denotes V_3, green denotes V_6, black denotes 0V, Purple some other voltage

R-String DAC



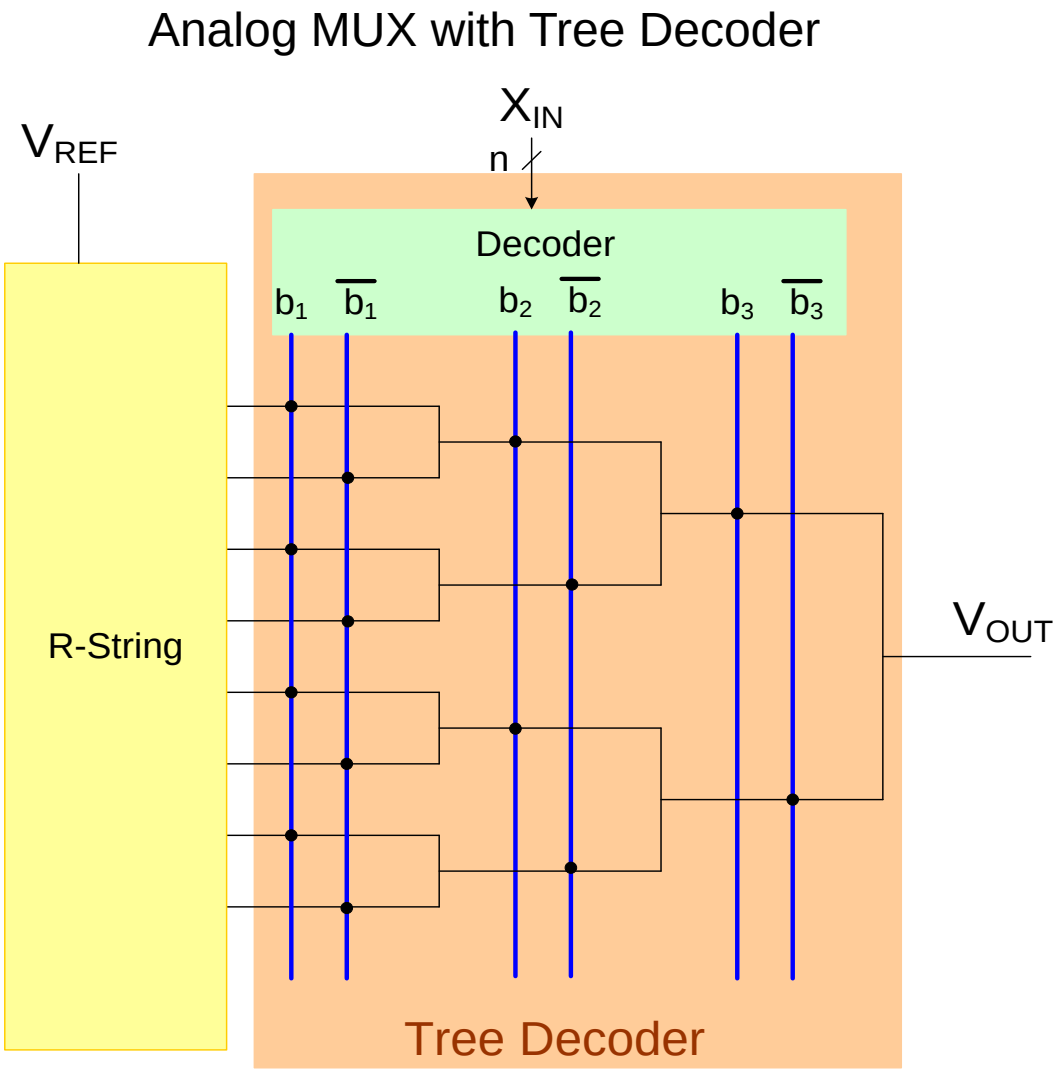
Tree-Decoder in Digital Domain

Single transistor used at each marked intersection to form PTL -AND gates

Do the resistors that form part of PTL dissipate any substantial power?

No because only one will be conducting for any DAC output

R-String DAC


Analog MUX with Tree Decoder
V_{REF}
X_{IN}
n
Decoder
b_1 $\overline{b_1}$ b_2 $\overline{b_2}$ b_3 $\overline{b_3}$
R-String
V_{OUT}
Tree Decoder

TEXAS INSTRUMENTS

DAC8560

SLAS464C – DECEMBER 2006 – REVISED JANUARY 2018

DAC8560 16-Bit, Ultra-Low Glitch, Voltage Output Digital-to-Analog Converter With 2.5-V, 2-ppm/°C Internal Reference

1 Features

- Relative Accuracy: 4 LSB
- Glitch Energy: 0.15 nV-s
- *Micro*Power Operation: 510 μA at 2.7 V
- Internal Reference:
  - 2.5-V Reference Voltage (Enabled by Default)
  - 0.02% Initial Accuracy
  - 2-ppm/°C Temperature Drift (Typical)
  - 5-ppm/°C Temperature Drift (Maximum)
  - 20-mA Sink/Source Capability
- Power-On Reset to Zero
- Power Supply: 2.7 V to 5.5 V
- 16-Bit Monotonic Over Temperature Range
- Settling Time: 10 μs to ±0.003% FSR
- Low-Power Serial Interface With Schmitt-Triggered Inputs
- On-Chip Output Buffer Amplifier With Rail-to-Rail Operation
- Power-Down Capability
- Drop-In Compatible With DAC8531/01 and DAC8550 /51
- Temperature Range: –40°C to +105°C
- Available in a Tiny 8-Pin VSSOP Package

3 Description

The DAC8560 is a low-power, voltage output, 16-bit digital-to-analog converter (DAC). The DAC8560 includes a 2.5-V, 2-ppm/°C internal reference (enabled by default), giving a full-scale output voltage range of 0 V to 2.5 V. The internal reference has an initial accuracy of 0.02% and can source up to 20 mA at the V_{REF} pin. The device is monotonic, provides very good linearity, and minimizes undesired code-to-code transient voltages (glitch). The DAC8560 uses a versatile 3-wire serial interface that operates at clock rates up to 30 MHz. It is compatible with standard SPI, QSPI, Microwire, and digital-signal-processor (DSP) interfaces.

The DAC8560 incorporates a power-on-reset (POR) circuit that ensures the DAC output powers up at zero scale and remains there until a valid code is written to the device. The DAC8560 contains a power-down feature, accessed over the serial interface, that reduces the current consumption of the device to 1.2 μA at 5 V.

The low-power consumption, internal reference, and small footprint make this device ideal for portable, battery-operated equipment. The power consumption is 2.6 mW at 5 V, reducing to 6 μW in power-down mode.

The DAC8560 is available in an 8-pin VSSOP package.

7.3.1 Digital-to-Analog Converter (DAC)

The DAC8560 architecture consists of a string DAC followed by an output buffer amplifier. Figure 63 shows a block diagram of the DAC architecture.

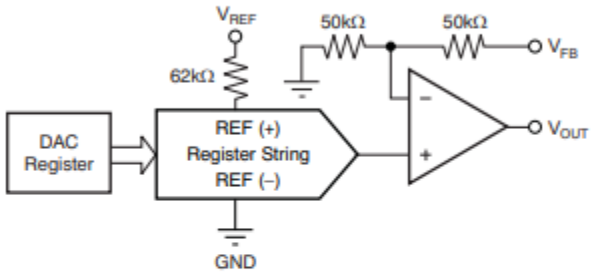


Figure 63. DAC8560 Architecture

The input coding to the DAC8560 is straight binary, so the ideal output voltage is given by:

$$V_{OUT} = \frac{D_{IN}}{65536} \times V_{REF} \quad (1)$$

where D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535.

7.3.2 Resistor String

The resistor string section is shown in Figure 64. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. It is monotonic because it is a string of resistors.

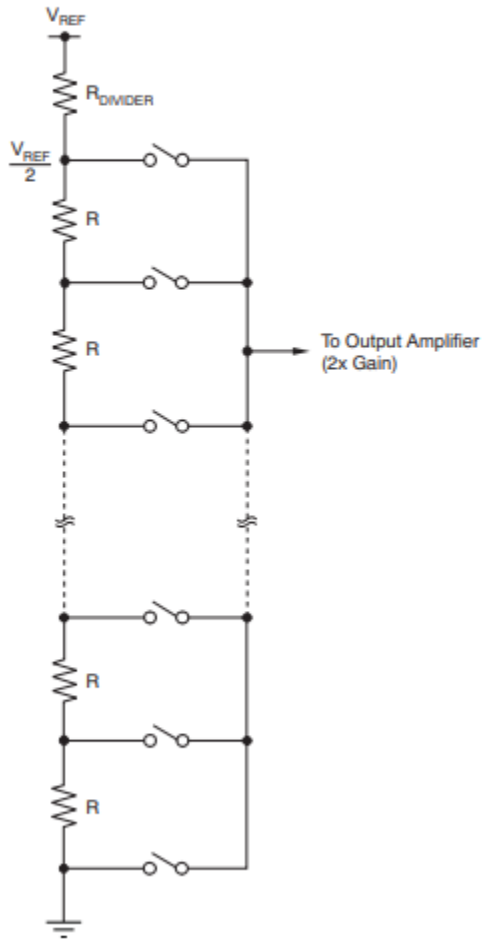


Figure 64. Resistor String

2 Applications

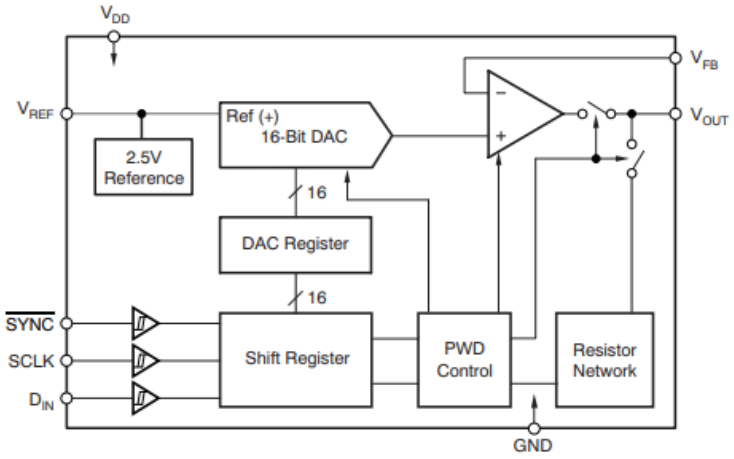
- Process Control
- Data Acquisition Systems
- Closed-Loop Servo-Control
- PC Peripherals
- Portable Instrumentation

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC8560	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



6.5 Electrical Characteristics

V_{DD} = 2.7 V to 5.5 V, –40°C to +105°C range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
Resolution			16			Bits
Relative accuracy	Measured by line passing through codes 485 and 64714	DAC8560A, DAC8560C		±4	±12	LSB
		DAC8560B, DAC8560D		±4	±8	LSB
Differential nonlinearity	16-bit Monotonic			±0.5	±1	LSB
Zero-code error	Measured by line passing through codes 485 and 64714.			±5	±12	mV
Full-scale error				±0.2	±0.5	% of FSR
Gain error				±0.05	±0.2	% of FSR
Zero-code error drift				±4		µV/°C
Gain temperature coefficient	V_{DD} = 5 V			±1		ppm of FSR/°C
	V_{DD} = 2.7 V			±3		
PSRR	Power supply rejection ratio	Output unloaded		1		mV/V
OUTPUT CHARACTERISTICS(2)						
Output voltage range			0		V_{REF}	V
Output voltage settling time	To ±0.003% FSR, 0200h to FD00h, R_L = 2 kΩ, 0 pF < C_L < 200 pF			8	10	µs
	R_L = 2 kΩ, C_L = 500 pF			12		
Slew rate				1.8		V/µs
Capacitive load stability	R_L = ∞			470		pF
	R_L = 2 kΩ			1000		
Code change glitch impulse	1 LSB change around major carry			0.15		nV-s
Digital feedthrough	SCLK toggling, $\overline{SYNC}$ high			0.15		nV-s
DC output impedance	At mid-code input			1		Ω
Short-circuit current	V_{DD} = 5 V			50		mA
	V_{DD} = 3 V			20		
Power-up time	Coming out of power-down mode V_{DD} = 5 V			2.5		µs
	Coming out of power-down mode V_{DD} = 3 V			5		
AC PERFORMANCE(2)						
SNR	T_A = 25°C, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz, 1st 19 harmonics removed for SNR calculation			88		dB
THD				–77		dB
SFDR				79		dB
SINAD				77		dB
DAC output noise density	T_A = 25°C, at mid-code input, f_{OUT} = 1 kHz			170		nV/√Hz
DAC output noise	T_A = 25°C, at mid-code input, 0.1 Hz to 10 Hz			50		μV_{PP}

(1) Linearity calculated using a reduced code range of 485 to 64714; output unloaded.
(2) Ensured by design and characterization, not production tested.

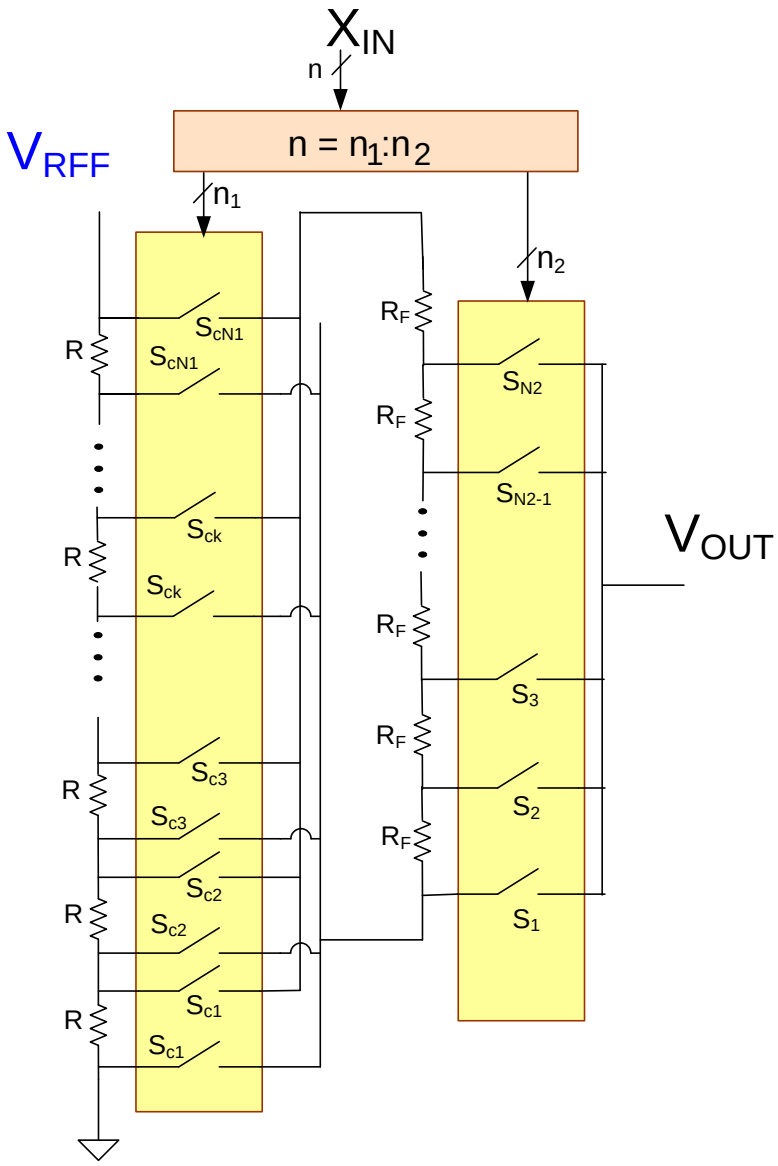
The DAC 8560

What is the INL performance of this DAC?

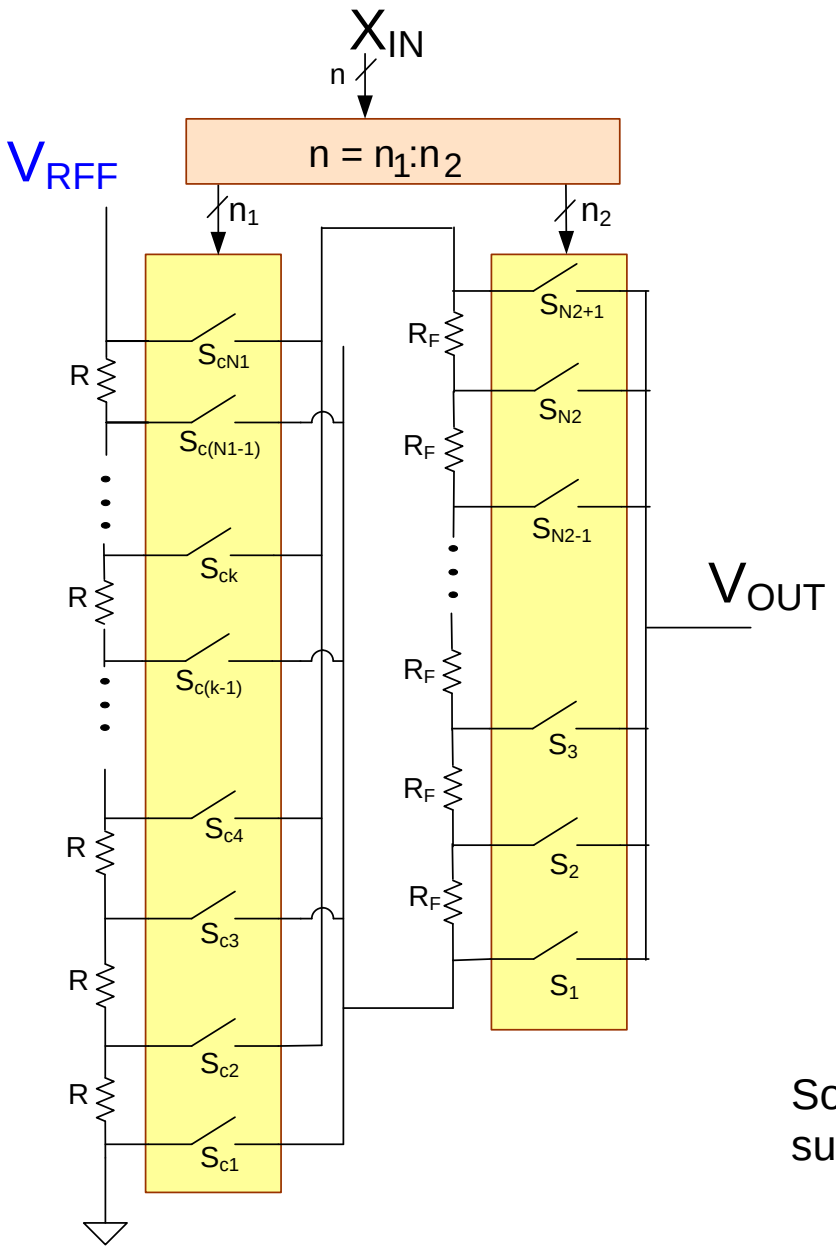
ENOB?

What is the spectral performance?

R-String DAC


X_IN
n
n = n1:n2
V_RFF
n1
n2
R
R
R
R
R
S_cN1
S_cN1
S_ck
S_ck
S_c3
S_c3
S_c2
S_c2
S_c1
S_c1
R_F
R_F
R_F
R_F
R_F
S_N2
S_N2-1
S_3
S_2
S_1
V_OUT

R-String DAC



Sometimes termed sub-divider, sub-range or dual-string DAC

Stay Safe and Stay Healthy !

End of Lecture 30